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IMPLEMENTATION OF DUAL STACK TECHNIQUE FOR REDUCING LEAKAGE AND DYNAMIC POWER

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Abstract- This paper deals with proposal of a new dual stack approach for reducing both leakage and dynamic powers. The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. As voltages scale downward with the geometries threshold voltages must also decrease to gain the performance advantages of the new technology but leakage current increases exponentially. Today leakage power has become an increasingly important issue in processor hardware and software design. It can be used in various applications like digital VLSI clocking system, buffers, registers, microprocessors etc. The leakage power increases as technology is scaled down. In this paper, we propose a new dual stack approach for reducing both leakage and dynamic powers. Moreover, the novel dual stack approach shows the least speed power product when compared to the existing methods. All well known approach is “Sleep” in this method we reduce leakage power. The proposed Dual Stack approach we reduce more power leakage. Dual Stack approach uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the Dual Stack portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit. The dual stack approach shows the least speed power product among all methods. The Dual Stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product.

Keywords -Leakage power, Dual Stack, Sub-threshold.

I. INTRODUCTION

Leakage power has been increasing exponentially with the technology scaling. In 90nm node, leakage power can be as much as 35% of chip power. Consequently, leakage power reduction becomes critical in low-power applications such as cell phone and handheld terminals. Power-gating is the most effective standby leakage reduction method recently developed. In the power gating, sleep transistors are used as switches to shut off power supplies to parts of a design in standby mode. Although the concept of the sleep transistor is simple, design of a correct and optimal sleep transistor is challenge because of many effects introduced by the sleep transistor on design performance, area, rout ability, overall power dissipation, and signal/power integrity. Currently, many of the effects have not been fully aware by designers. This could result in improper sleeper transistor design that would either fail to meet power reduction target when silicon is back or cause chip malfunction due to serious power integrity problems introduced. We have carried out comprehensive investigations on various effects of sleep transistor design and implementations on chip performance, power, area and reliability.

In this paper, we shall describe a number of critical considerations in the sleep transistor design and implementation including header or footer switch selection, sleep transistor distribution choices and sleep transistor gate length, width and body bias optimization for area, leakage and efficiency. A sleep transistor is referred to either a PMOS or NMOS high transistor that connects permanent power supply to circuit power supply which is commonly called “virtual power supply”. The sleep transistor is controlled by a power management unit to switch on and off power supply to the circuit. The PMOS sleep transistor is used to switch VDD supply and hence is named “header switch”. The NMOS sleep transistor controls VSS supply and hence is called “footer switch”. Low power has emerged as a principal theme in today’s electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. Two components determine the power consumption in a CMOS circuit.

Static power: Includes sub-threshold leakage, drain junction leakage and gate leakage due to tunneling.
Among these, sub threshold leakage is the most prominent one. 

**Dynamic power**: Includes charging and discharging power and short circuit power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases. Furthermore, the structure of the short channel device lowers the threshold voltage even lower. So it is becoming more and more important to reduce leakage power as well as dynamic power. There are several VLSI techniques for reducing leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit its application. In this paper, we propose a novel dual stack technique that reduces not only leakage power but also dynamic power. We Summarized and compared the previous techniques with our new approach.

**A. AIM OF THE PAPER**

Today leakage power has become an increasingly important issue in processor hardware and software design. The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. In this paper, we shall describe a number of critical considerations in the sleep transistor design and implementation including header or footer switch selection, sleep transistor distribution choices and sleep transistor gate length, width and body bias optimization for area, leakage and efficiency.

In this paper, we propose a novel dual stack technique that reduces not only leakage power but also dynamic power. We Summarized and compared the previous techniques with our new approach. We provide novel circuit structure named “Dual stack” as a new remedy for designers in terms of static power and dynamic powers. Unlike the sleep transistor technique, the dual stack technique retains the original state. The dual stack approach shows the least speed power product among all methods. Therefore, the dual stack technique provides new ways to designers who require ultra-low leakage power consumption with much less speed power product.

**B. METHODOLOGY**

Complementary metal-oxide-semiconductor is a technology for constructing integrated circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips.

**C. SIGNIFICANCE OF WORK**

**Power Leakage Technique**

There are several VLSI techniques for reducing leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit its application. In this paper, we propose a novel dual stack technique that reduces not only leakage power but also dynamic power.

The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to significant growth in power density. Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. As voltages scale downward with the geometries threshold voltages must also decrease to gain the performance advantages of the new technology but leakage current increases exponentially. Today leakage power has become an increasingly important issue in processor hardware and software design. In 65 nm and below technologies, leakage accounts for 30-40% of processor power. In this paper, we propose a new dual stack approach for reducing both leakage and dynamic powers. Moreover, the dual stack approach shows the least speed power product when compared to the existing methods.

**II. LITERATURE SURVEY**

Sub-threshold leakage power increases exponentially as threshold voltage decreases. Furthermore, the structure of the short channel device lowers the threshold voltage even lower. So it is becoming more and more important to reduce leakage power as well as dynamic power. There are several VLSI techniques for reducing leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit its application. In this paper, we propose a novel dual stack technique that reduces not only leakage power but also
dynamic power. We summarized and compared the previous techniques with our new approach. It enumerates low power, high speed design of flip-flop having less number of transistors and only one transistor being clocked by short pulse train which is true single phase clocking (TSPC) flip-flop. Compared to Conventional flip-flop, it has 5 Transistors and one transistor clocked, thus has lesser size and lesser power consumption. It can be used in various applications like digital VLSI clocking system, buffers, registers, microprocessors etc. The analysis for various flip flops and latches for power dissipation and propagation delays at 0.13μm and 0.35μm technologies is carried out. The leakage power increases as technology is scaled down. Thereby comparison of different conventional flip-flops and TSPC flip-flop in terms of power consumption, propagation delays and product of power dissipation and propagation delay with SPICE simulation results is presented.

A. TECHNIQUES FOR LEAKAGE POWER REDUCTION

Techniques for leakage power reduction can be grouped into two categories: state-preserving techniques where circuit state is retained and state-destructive techniques where the current Boolean output value of the circuit might be lost. A state-preserving technique has an advantage over a state-destructive technique in that with a state-preserving technique the circuitry can resume operation at a point much later in time without having to somehow regenerate state. There are several VLSI techniques for reducing leakage power. Each technique provides an efficient way to reduce leakage power. They are:
1. Sleep Method
2. Sleepy Stack Method
3. Dual Sleep Method
4. Dual Stack Approach Method

Existing Method

While Designing of Inverters we have Techniques for leakage power reduction can be grouped into two categories: state-preserving techniques, state-destructive techniques

A state-preserving technique has an advantage over a state-destructive technique in that with a state-preserving technique the circuitry can resume operation at a point much later in time without having to somehow regenerate state. All well known approach is “Sleep” in this method we reduce leakage power. The proposed Dual Sleep approach we reduce more power leakage.

Proposed Method

Dual stack approach uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual stack portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit.

Leakage Power Analysis

Minimization power consumption is essential for high performance VLSI systems. In digital CMOS circuits there are three sources of power dissipation, the first is due to signal transition, the second comes from short circuit current which flows directly from supply to ground terminal and the last is due to leakage currents. As technology scales down the short circuit power becomes comparable to dynamic power dissipation. Furthermore, the leakage power also becomes highly significant. High leakage current is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length and gate oxide thickness are reduced. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power especially for low-power applications. Multivariable Threshold voltage CMOS (MTCMOS) and voltage scaling are two of the methods to reduce power.

III. SYSTEM DEVELOPMENT

Sleep Method

In the sleep approach, a "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and a "sleep" NMOS transistor is placed between the pull-down network and Ground. These sleep transistors turn off the circuit by cutting off the power rails. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively. However, output will be floating after sleep mode, so the technique results in destruction of state plus a floating output voltage. The circuit is connected as shown in the figure 1.

Figure 1: Sleep method
Figure 2: Circuit diagram of an exor gate in sleep method.

Sleepy Stack Method

Another technique for leakage power reduction is the stack approach, which forces a Stack effect by breaking down an existing transistor into two half size transistors. The divided transistors increase delay significantly and could limit the usefulness of the approach. The sleepy stack approach combines the sleep and stack approaches. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. The circuit is connected as shown in the figure 2.

Figure 3: Sleepy stacky method

Dual Sleep Method

Another technique called Dual sleep approach uses the advantage of using the two extra pull-up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. Since the dual sleep portion can be made common to all logic circuitry, less number of transistors is needed to apply a certain logic circuit. The circuit is connected as shown in the figure below.

Figure 5: Dual Sleep method
In this section, the structure and operation of our novel low-leakage-power design is described. It is also compared with well-known previous approaches, i.e., the sleepy stack, dual sleep and sleep transistor method. Here we use 2 PMOS in the pull-down network and 2 NMOS in the pull up network. The transistors are held in reverse body bias. As a result their threshold is high. High threshold voltage causes low leakage current and hence low leakage power. The circuit is connected as shown in the figure below.

**IV. PERFORMANCE ANALYSIS**

Leakage power has been increasing exponentially with the technology scaling. Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. Consequently, leakage power reduction becomes critical in low-power applications such as cell phone and handheld terminals. The simulation parameters have been analyzed with the help of the Micro wind tool and DSCH for the schematic verification.

**Connecting Procedure**

Instantiate NMOS or PMOS transistors from the symbol library and place them in the editor window. An exor gate is designed by using CMOS transistors. It is designed by using four inverters, two AND gates and one OR gate. Connect $V_{DD}$ and GND to the schematic. Connect input button and output LED. The simulation output can be observed as a waveform after the application of the inputs as above. Click on the timing diagram icon in the icon menu to see the timing diagram of the input and output waveforms.

*When the inputs are $a=0$, $b=1$; the output is $c=1$;*  
*When the inputs are $a=0$, $b=0$ the output is $c=0$;*  
*When the inputs are $a=1$, $b=0$ the output is $c=1$;*

The red color at the input and output in the below simulation results indicate logic ‘1’ and the black color at the input and output indicates logic ‘0’. Below is the simulation results obtained after the application of inputs.
(a) Simulation result of Sleep method
When the input is $a=0$, $b=1$ the output is $c=1$;

Figure 9: Simulation Result of Sleep method for inputs $a=0$, $b=1$;

When the input is $a=0$, $b=0$ the output is $c=0$;
When the input is $a=1$, $b=0$ the output is $c=1$;

Fig 10 Simulation Result of Sleep method for inputs $a=1$, $b=0$;

(b) Simulation Result- Sleepy Stack Method
When the input is $a=0$, $b=1$ the output is $c=1$;

Figure 11: Simulation Result of Sleepy Stack method for inputs $a=0$, $b=1$;

When the input is $a=1$, $b=0$ the output is $c=1$;

Figure 12: Simulation Result of Sleepy Stack method for inputs $a=1$, $b=0$;

(c) Simulation Result- Dual Sleep Method
When the input is $a=1$, $b=0$ the output is $c=1$;

Figure 13: Simulation Result of Dual Sleep method for inputs $a=1$, $b=0$;

When the input is $a=0$, $b=1$ the output is $c=1$;

Figure 14: Simulation Result of Dual Sleep method for inputs $a=0$, $b=1$;

(d) Simulation Result- Dual Stack Approach Method
When the input is $a=0$, $b=1$ the output is $c=1$;
Figure 15: Simulation Result of Dual Stack Approach method for inputs a=0, b=1;

When the input is a=0, b=0 the output is c=0;

Figure 16: Simulation Result of Dual Stack Approach method for inputs a=0, b=0;

When the input is a=1, b=0 the output is c=1;

Figure 17: Simulation Result of Dual Stack Approach method for inputs a=1, b=0;

Power Consumption:

Below are the power consumption values for different methods at the CMOS level-70 nm. We observe that power consumed for dual stack approach method is less than all other methods.

(a) Power Consumption-Sleep Method

Figure 18: Power Consumption of Sleep method CMOS level-70nm; power=6.668µw

(b) Power Consumption-Sleepy Stack Method

Figure 19: Power Consumption of Sleepy Stack method CMOS level-70nm; power=5.424µw
From the above tabular form we observe that power is mostly reduced in dual stack approach method. Therefore, the dual stack technique provides a new ways to designers who require ultra-low leakage power consumption with much less speed power product.

V. CONCLUSION

In nanometer scale CMOS technology, sub threshold leakage power consumption is a great challenge. Although previous approaches are effective in some ways, no perfect solution for reducing leakage power consumption is yet known. Therefore, designers choose techniques based upon technology and design criteria. We provide novel circuit named “Dual Stack” as a new remedy for designers in terms of static power and dynamic powers. Unlike the sleep transistors technique, the dual stack technique retains the original state. The dual stack technique shows the least speed power product among all methods. Therefore, the dual stack technique provides a new ways to designers who require ultra-low leakage power consumption with much less speed power product. Supervisory and leakage powers generated by input output control systems. Such current can cause problems when interacting with new low power components such as solenoid valves and sensors. These are used to open solenoid valves and larger balls or butterfly valves for fail safe air release in low power reduction techniques. Core memory cells changing state. Leakage power is becoming a more significant component of the total memory power at 40 and 32 nm.

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