

Z-source inverter topologies with switched Z-impedance networks: A review

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Abstract

The Z-source inverter is one of the most interesting power electronic converters. Over the past decades, research and development have been in high demand to meet the challenges for improving the converter performance with reduced weight and cost while having high efficiency along with high gain or boost factor. Since the inception, tons of resolutions, customizations, and improvements have appeared to achieve these performance goals. To overcome the most common drawback, i.e. the low boost factor of classical Z-source inverters, the switched inductor/capacitor and switched boost Z-source inverter topologies have become predominant in the recent epoch. Furthermore, the higher component voltage stress, discontinuous input current, and high inrush start-up current issues have also been addressed and solved in various literature as part of this topical advancement. In this study, a comprehensive review of various switched impedance network-based Z-source inverter topologies has been accomplished for providing a quick report to researchers and engineers so that they can consider this as a one-stop solution for selecting inverters from this group. The overall study covers the methodology, features, and relevant important results of the latest switched Z-source inverter models in order to demonstrate the coordination between pitfalls and improvements.

1 | INTRODUCTION

In recent years, the Z-source inverter (ZSI) has become one of the most promising buck-boost converters in power electronic (PE) applications [1, 2]. Being an emerging topology, the ZSI provides an attractive feature for one-stage power conversion with simultaneous buck-boost ability. The main ZSI converter configuration is constituted with one diode, two capacitors, two inductors, and six semiconductor switches. This classical Z-source converter is an X shape two-port circuit where the LC paired network, i.e. the impedance network is placed between the inverter bridge and input DC source as shown in Figure 1. The ZSI purposely utilizes the shoot-through (ST) states to boost the DC link voltage of the inverter which is impermissible in traditional voltage source inverters (VSIs). The design and parametric analysis have been presented in [3–5]. Moreover, this single-stage boosting phenomenon reduces the system cost and size as well as increases the reliability and efficiency

of the PE converter [6]. As indicated in [6], it can be clearly seen that the ZSI performs better than the boost converter in series with a VSI (BC-VSI) in terms of the size, cost, efficiency, and reliability. However, the BC-VSI performs better in terms of the efficiency depending on the control strategy [7] and the consideration of the control strategy is out of the scope of this work. Various applications such as photovoltaic (PV) [8–11], wind [14], fuel cells [12, 13], and grid integration [15–18] of traditional ZSIs have been studied where the ZSI has proved its significance by acting as a reliable PE converter. Furthermore, the ZSI plays key role in the field of electric motor drives [19], DC circuit breakers [20], and hybrid electric vehicles [21] applications.

Despite the aforementioned merits, the classical voltage-fed ZSI suffers from the low boost factor, high start-up inrush current, discontinuous input current, high capacitor voltage and semiconductor switch voltage stress; and the absence of common ground between the inverter and source. Thus,

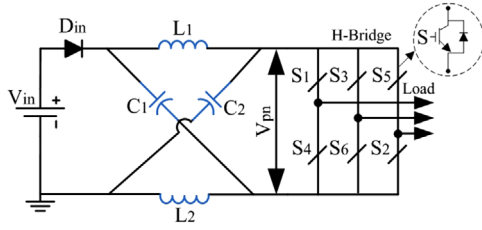


FIGURE 1 Classical Z-source inverter

the converter is unable to perform up to the expected level. Hence, all these factors motivated the researchers to stretch out the scope to bring further improvements on the basic ZSI topology [22]. Since the inception of ZSIs, several topological improvements have appeared in [23–28] where the basic impedance network of the conventional ZSI is rearranged to overcome some specific problems. In all these developments, each shows its features and drawbacks in a parallel manner. Primarily, most of these have reduced the voltage stress of the component and improved the input current profile. However, the boost inversion capability of traditional ZSIs remains the same for all these configurations. Hence, as a research hotspot, the investigation was carried out to further improve the boost factor of ZSIs, and in 2010, a completely new structure of ZSI topology was proposed with a switched inductor (SL) technique by Zohu *et al.* [29, 30]. The topology was a three-phase two-level voltage-fed inverter like the traditional ZSI. The technique was taken up from the previously designed switched-capacitor (SC), SL, and hybrid SC/SL-based DC–DC converters [31, 32].

Therefore, the combination of the basic ZSI impedance network and the advanced SL cells are employed in [30] and the first basic SL-ZSI structure has been formed as shown in Figure 2(a) which provides an excellent voltage boost and inversion ability that ultimately improves the performance and promotes its industrial applications. In the later phase, the SL technique was applied in [33–35] to investigate the performance of quasi, embedded, and improved structures of the ZSI, respectively (see

Figures 6, 8, and 9). The main characteristics and the operation of ST and non-shoot-through (nST) states of the classical SL-ZSI are summarized as follows:

1. The two SL cells, namely $(L_1 - L_3 - D_1 - D_2 - D_3)$ and $(L_2 - L_4 - D_4 - D_5 - D_6)$, for the upper and lower cells, respectively, are reconfigured in the primary X-shaped ZSI structure.
2. The boost factor has been uplifted from $1/(1 - D_S)$ to $(1 + D_S)/(1 - 3D_S)$.
3. Only six diodes (D_1, D_2, D_3, D_4, D_5 , and D_6) and two inductors (L_3 and L_4) are added in the network.
4. The output power quality improvement is ensured with a high modulation index and low ST duty ratio.
5. The structure is expansible for further structural improvement.

1.1 | Operating principle of the basic SL-ZSI

The concept of the SL-ZSI can be applied to any DC–DC, DC–AC, AC–DC, and AC–AC power conversions [22]. All traditional modulation techniques as summarized in [36] and the improved versions as studied in [37–39] are generally applicable for the ST operation of the SL-ZSI topology. In this study, the most commonly used simple boost control (SBC) modulation technique has been adopted for the simplicity, as shown in Figure 3. In addition to the traditional three-phase sinusoidal pulsewidth modulation signals, a positive DC signal V_p and a negative DC signal V_n are inserted to generate the additional ST pulses. The operating principle and fundamental boosting concept of the SL-ZSI can be understood by following Figure 2. The energy storing and transferring take place between capacitors and DC-bus bar through the switching action of the impedance circuit. The operation of the SL-ZSI is the same as the classical ZSI and can be explained by the same ST and nST modes shown in Figure 2(b) and (c), respectively.

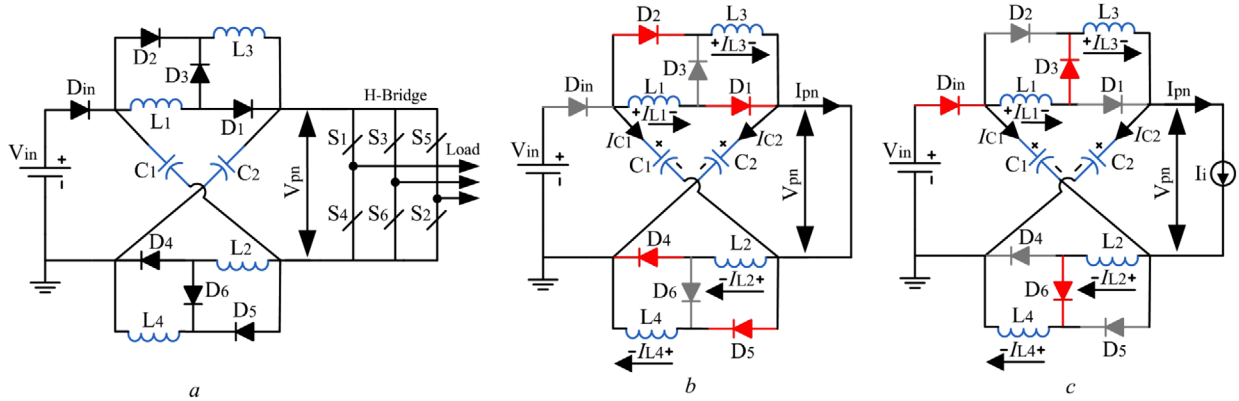


FIGURE 2 Classical switched inductor ZSI

(a) SL-ZSI; (b) ST equivalent circuit; (c) nST equivalent circuit

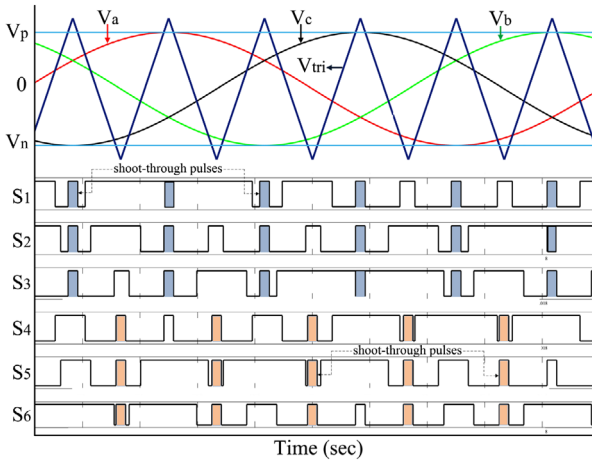


FIGURE 3 Simple boost modulation control [36]

1.1.1 | Shoot-through mode

During this state, the output side, i.e. the inverter bridge terminals of the impedance network are short-circuited by the combination of the semiconductor switches (S_1, S_2, S_3, S_4, S_5 , and S_6). The input diode D_{in} becomes OFF and the energy flows from capacitors to inductors during this time interval. The stored energy is transferred to the load in the following active switching states of the inverter and the input diode conducts in this stage. Furthermore, diodes D_1 and D_2 are ON in the top SL cell and D_3 is OFF during this state. The capacitor C_1 charges inductors L_1 and L_3 in parallel. Similarly, in the bottom SL cell, diodes D_4 and D_5 become ON and D_6 is OFF. At this moment, capacitor C_2 charges inductors L_2 and L_4 in parallel. The function of both SL cells is to absorb the stored energy from capacitors.

1.1.2 | Non-shoot-through mode

This state works in the conventional switching fashion with six active and two zero states of the main circuit. During the energy transfer to the load, the input diode D_{in} along with diodes D_3 and D_6 in top and bottom SL becomes ON. The inductors L_1 and L_2 are connected in series and the same connection is followed for the inductors L_3 and L_4 . On the other hand, diodes D_1, D_2 and D_4, D_5 on both SL cells are OFF. At the same time, the capacitor C_1 gets charged by V_{in} through the path in the bottom SL cell and the capacitor C_2 is charged by V_{in} via the path in the top SL cell.

An expression of calculating the peak DC-link voltage is resulted by the average of these two switching conditions and can be expressed as $V_{pn} = (1 + D_S) \cdot V_{in} / (1 - 3D_S)$, where D_S is the ST time interval and $\hat{V}_{pn}$ is the peak inverter DC link voltage. The SL-ZSI has nine permissible switching states like traditional ZSI, including the additional ST state. During the zero states, all three upper or lower inverter switches are simultaneously turned ON and impress zero voltage across the output

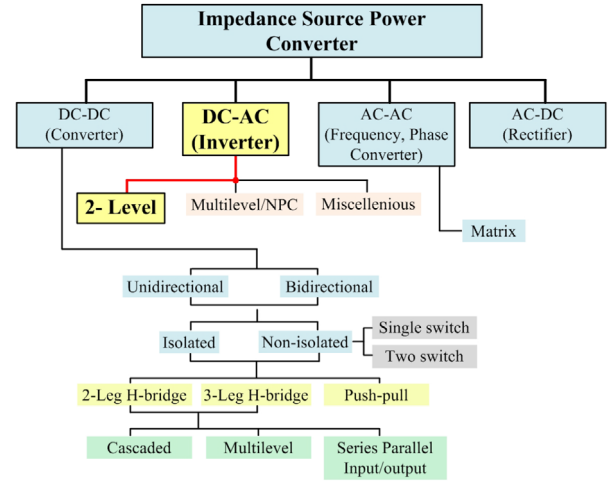


FIGURE 4 Classifications of impedance source converters [40]

load. The ST pulses are inserted during the zero states having the same zero voltage effect on the output and boosts the output voltage.

From the viewpoint of electric power conversion categories, as shown in Figure 4, the SL-ZSI network is configurable to systems with any conversion strategies, i.e. for DC-DC, DC-AC, AC-DC, and AC-AC systems. Although SL-ZSI can be configured for VSIs or CSIs for two-level and multilevel configurations and further non-isolated and isolated structure, this article concentrated on the two-level voltage source non-isolated SL-ZSI topology and its off-springs for precisely framing out the state of developments. Note that all non-active and active switch impedance networks are considered in this study under the category of switched Z-impedance topologies. The non-active switch impedance networks are developed based on the capacitor, inductor, and diodes in its Z network while the active switch impedance network contains the additional semiconductor switch in the structure. Furthermore, there is no hard and fast rule for naming any topologies which fall under any of these two types. Ideally, the nomenclature of the non-active switch topologies follow the classical ZSI and the active switch topologies follow the switched boost inverter (SBI), respectively.

1.2 | Status and application of classical SL-ZSIs

Research activities on switched inductor/capacitor-based ZSIs have gained much popularity since it was first introduced in 2010 and the number of new topologies and improvements has been increased drastically. According to the experts and pioneers, the demand and interest have encouraged researchers to investigate new ideas and solutions using this emerging technology [41, 42]. Although there are various structures in the present literature and each one of them has their unique feature, almost all these topologies have pros and cons in their functionalities.

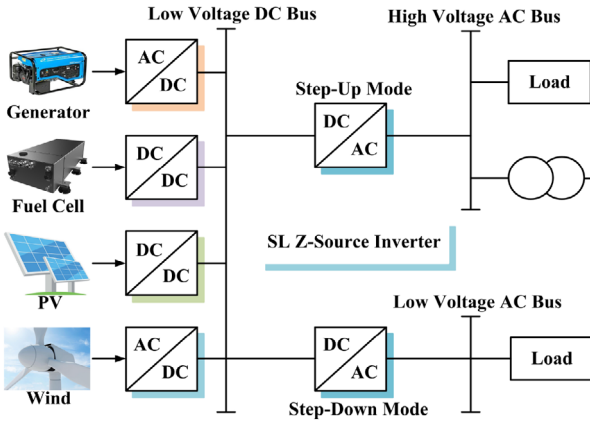


FIGURE 5 General applications of SL-ZSI [30]

Still now, there is no single structure which fits all solutions. It is expected that the upcoming topologies will continuously strive to meet and improve the inverter performance [43]. The rigorous review of different SBI/ZSI topologies is presented in [43, 44]. The novelty of this review paper can be highlighted in terms of the following three key points while comparing with [43] and [44]:

1. The term 'SWITCHED' in both proposed and in [43] is unfixed. In the proposed paper, this term refers to any switched configurations of ZSI/SBI impedance networks (e.g. switched inductors, switched capacitors, diode assisted, with active switch components etc.). On the other hand, [43] directs the topologies with active switch impedance networks.
2. Though four basic switched structured topologies (e.g. SL-ZSI, SL-qZSI, SL-EZSI, and SL-IZSI) as presented previously in the proposed paper are similar to that of [44], these will be included in Section 2 to maintain the chronological flow.
3. The proposed paper covers four new two symmetric and highly significant topologies, i.e. EB-ZSI, EB-qZSI, MCA-ZSI, and ESL-qZSI without active switch in the impedance network (see Section 3) while [43] only considers the SBI topologies and these four basic topologies and their descendants are not covered in any of these existing review papers. Though [43] and proposed papers cover SBI topologies, the proposed paper comprehensively considers all state-of-the-art topologies as compared to [43].

Since the renewable energy sources such as PV, wind, and fuel cell are intermittent in nature, the SL-ZSI shown in Figure 5 is deployed with such sources to harness electric energy due to its strong buck-boost ability.

The paper provides a comprehensive review by focusing on two-level transformerless switched impedance ZSI topologies which are organized as follows. Section 2 describes various topologies of the fundamental SL-ZSI while Section 3 provides the topological development of two switched extended SC/SC

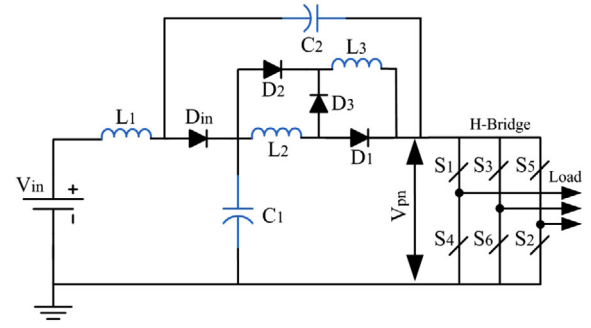


FIGURE 6 Basic switched inductor quasi ZSI (SLq-ZSI)

ZSIs. An active switch component-based SBI is explained in Section 4. In Section 5, the challenges and future directions related to ZSI systems are discussed and, finally, the work is concluded in Section 6.

2 | TOPOLOGY IMPROVEMENTS OF BASIC SL-ZSIs

A wide range of different SL-ZSIs are derived mainly with the help of quasi-type ZSI, embedded-type ZSI, and improved-type ZSI skeletons. The modification is done basically by rearranging the existing or adding additional components on the basic structure. Each topology provides distinct features and particular needs related to its applications. The new impedance networks are being developed for four main reasons [40]:

1. extending the range of inverter voltage gain;
2. achieving the high-density power conversion;
3. reducing component count and cost; and
4. achieving application-oriented optimization and improvement.

Different structures have been investigated using the aforementioned three ZSI skeletons and the topological improvements have been briefly discussed in the following subsections.

2.1 | SL-quasi ZSIs (SL-qZSIs)

The quasi skeleton is the first modification of the classical ZSI which holds various features. In [33], the q-ZSI is configured into an SL-quasi structure by imposing one SL cell ($L_2 - L_3 - D_1 - D_2 - D_3$) into the impedance network shown in Figure 6. Unlike the classical SL-ZSI, with the direct connection of the inductor (L_1) with the input DC source, the drawn input current becomes continuous and reduces the stress of the source. The overall impedance network of the SL-qZSI is connected in series with the DC-side, and hence, the lower capacitor voltage stress improves the performance of the inverter and provides a common ground as well. The common ground reduces the

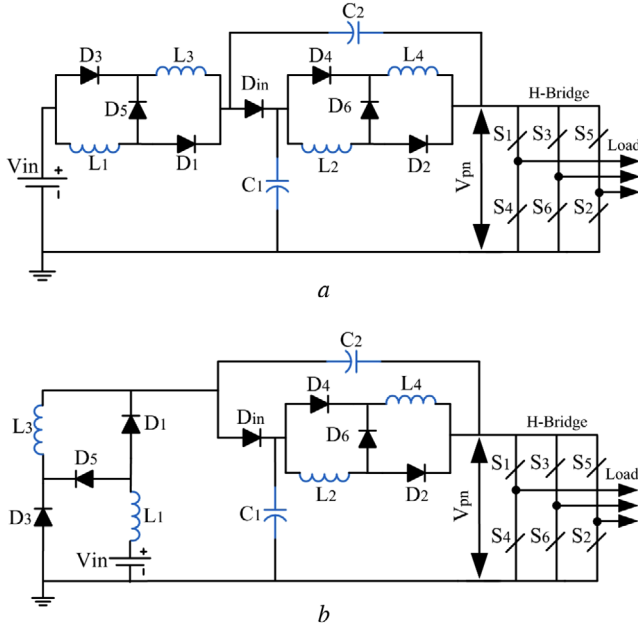


FIGURE 7 SL-qZSI topologies

(a) rSL-qZSI, (b) cSL-qZSI

leakage current in PV applications which is an added advantage of any topology [45–47]. By following this trend, two new structures, namely, ripple current input qZSI (rSL-qZSI) and continuous current input qZSI (cSL-qZSI), are introduced in [48] where two separate SL cells are composed comprising two extra inductors and three diodes in the impedance network. Figure 7(a) and (b) shows the configuration of these topologies. Both inverters possess high voltage boost inversion ability and low switch voltage stress on semiconductor switches during the operation. The start-up inrush current is successfully suppressed by these inverters, which is not possible in the traditional SL-ZSI. Compared to rSL-ZSI, the cSL-ZSI contains less ripple, and hence, shows better performance. Apart from these studies, several other SL-qZIs were studied in [49–51] to provide parallel solutions for overcoming these drawbacks.

2.2 | SL-embedded ZSIs (SL-EZSIs)

The basic embedded ZSI was first introduced due to its filter function by which the input current can be drawn smoothly and continuously that makes it appropriate for PV and fuel cell applications [53]. Figure 8(a) shows the SL-based embedded ZSI structure (SL-EZSI), where two isolated input DC supplies are placed in series with the SL cells [34]. In [52], two new structures, ripple current input (rESL-ZSI) and continuous current input (cESL-ZSI) [see Figure 8(b) and (c)], are proposed where both of them successfully attained all features of [48]. It can be observed that both topologies have the same component

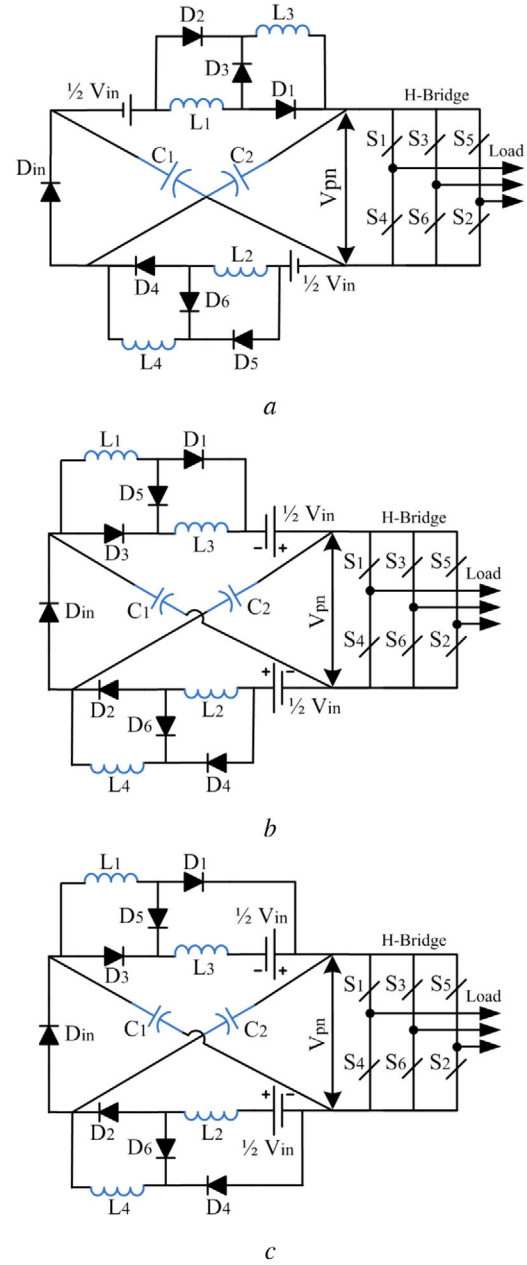


FIGURE 8 Basic switched inductor-embedded ZSI

(a) ESL-ZSI, (b) rESL-ZSI, (c) cESL-ZSI

count but the DC source is split to improve the functionality of converters.

2.3 | SL-improved ZSIs (SL-IZSIs)

Based on the concept of the basic improved ZSI skeleton, the SL-improved ZSI (SL-IZSI) topology, as shown in Figure 9, was studied in [35]. In the SL-IZSI, the same advantages are prevailed with the less number of DC sources as compared

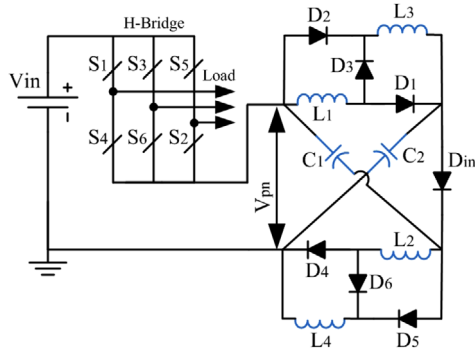


FIGURE 9 Basic switched inductor improved ZSI (SL-IZSI)

to [34]. Moreover, a common ground is shared between the input DC and inverter bridge which has added an extra advantage of removing the common-mode noise in the system. In parallel to this fundamental topology, many other modifications were brought out in [54–61] based on the coupled inductors and transformer to resolve the common issues. However, the proper operation of these topologies heavily relies on the perfect magnetic coupling, i.e. the design of the transformer. In these transformer-based topologies, the switching current during the transient events generally produces high voltage spikes due to improper couplings of magnetic components, and hence, the inverter circuitry might be damaged. However, in this study, only the non-isolated, i.e. transformerless switched Z-impedance ZSI topologies are focused. Furthermore, the two symmetric switched impedance network-based ZSI topologies are discussed in the following section.

3 | TWO SYMMETRIC IMPEDANCE NETWORK-BASED SL/SC ZSIs

In recent years, the trend of the high voltage boost technique is drifting towards the use of two combined Z-impedance networks having additional capacitors, inductors, and diodes. Parallel to the high voltage boost feature, another main motivation of this idea is to drive the ZSI with higher modulation index to improve the output voltage waveform [62]. Such kind of structures use a low ST duty ratio and help to significantly increase the modulation index. Hence, the vigorous effort is being paid in this area to properly tackle the existing problems. The following subsections describe the methodology and features of different two symmetric ZSI networks.

3.1 | Enhanced boost ZSIs (EB-ZSIs)

An enhanced boost ZSI (EB-ZSI) as shown in Figure 10 is presented in [63] where the boost factor is further stepped up than [30] by using two combined Z-impedance networks. This topology introduces the fundamental concept of combining two Z-impedance networks to improve the boost factor. Although two more additional capacitors (C_3 and C_4) are used in [63], the

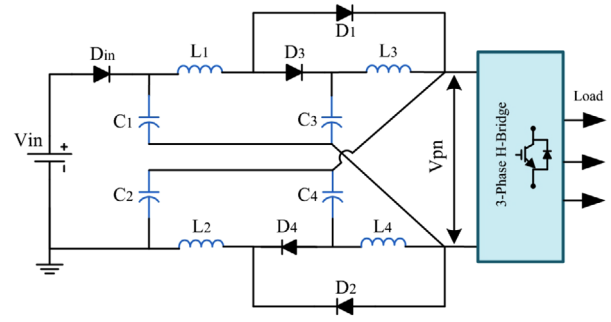


FIGURE 10 Basic enhanced boost ZSI (EB-ZSI)

number of diode count is less than the basic SL-ZSI structure. The voltage stresses on the capacitors are high and even more than the traditional ZSI; thus, the low voltage stress feature is absent in this topology. Furthermore, the high inrush start-up current is severe in EB-ZSI, which leads to the risk of damaging the inverter circuitry. To overcome the issues associated with the basic EB-ZSI, several configurations have been proposed in [64–66] [see Figure 11(a)–(d)] where the position of the components inside the network is rearranged without adding any extra components. From Figure 11(b)–(d), it can be seen that the input DC source is mainly split into two halves and distributed inside the network that significantly reduces the inrush current. Figure 11(a) followed the basic improved ZSI strategy where the position of the inverter bridge is changed to reduce the input current rush and capacitor voltage stress. However, the boost factor remains the same as of [63] which has stepped up to a new level than the SL-ZSI and can be fruitful for the high-voltage boost renewable energy applications.

3.2 | Enhanced boost quasi ZSIs (EB-qZSIs)

In [67, 68], the EB-ZSI structure is configured into the quasi EB-ZSI [see Figure 12(a) and (b)] and attained two different configurations of continuous input current (CIC) and discontinuous input current (DIC) EB-qZSIs. Figure 12(a) shows the CIC configuration which is achieved by connecting the negative side of the capacitor C_3 with the negative side of input DC supply. On the other hand, Figure 12(b) shows the DIC configuration where the negative side of the capacitor C_3 is connected with the positive side of the input DC source. Having the same number of components in the impedance network, the EB-qZSI has archived less capacitor voltage stress, reduced start-up inrush current, and common ground facility in its structure. In [69], a further modification in the capacitor connection provides two CIC configurations of the EB-qZSI [see Figure 12(c) and (d)] that have superior performance than even EB-qZSI topologies. Another combined two-quasi Z impedance topology (see Figure 13) was studied in [70, 71] where the number of passive components is the same as in [68] with the same boost ability but the efficiency of the inverter is proved to be higher than in [68].

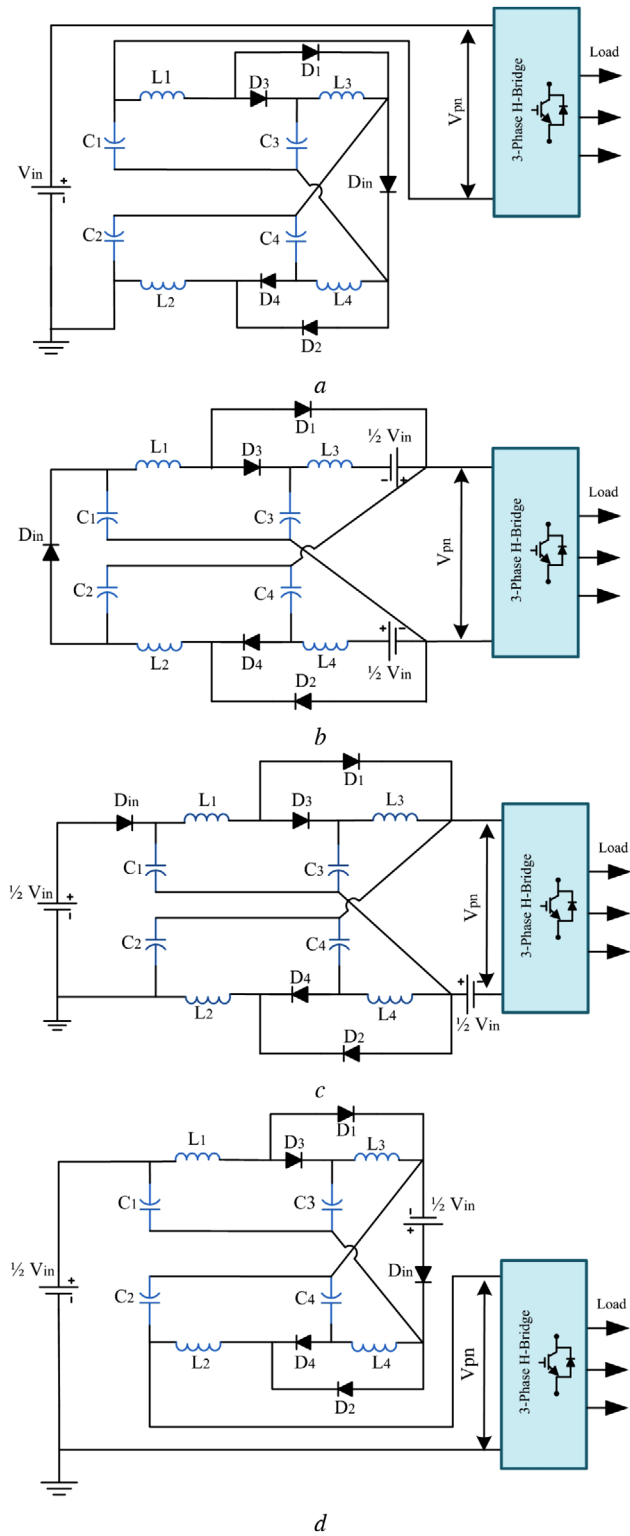


FIGURE 11 Different EB-ZSI topologies

(a) EBI-ZSI, (b) EEB-ZSI, (c) EBM-ZSI, (d) IEBM-ZSI

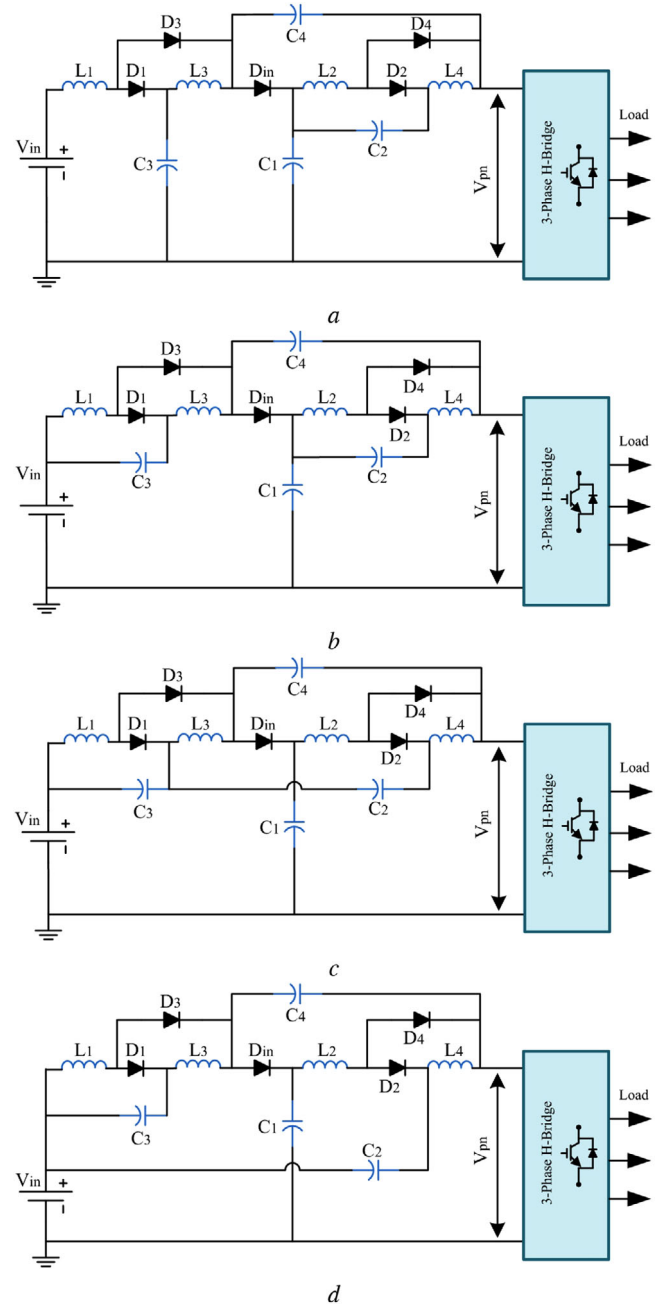


FIGURE 12 Different EB-qZSI topologies

(a) (CIC) EB-qZSI, (b) (DIC) EB-qZSI, (c) (CIC) EB-qZSI-C1, (d) (CIC) EB-qZSI-C2

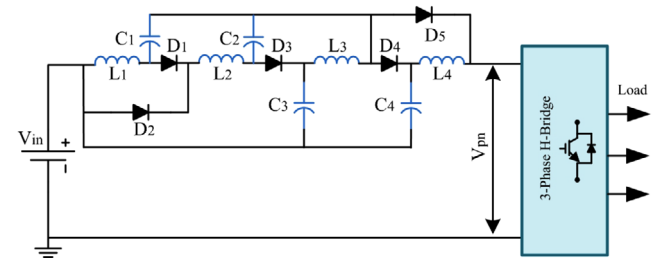


FIGURE 13 Enhanced boost two quasi ZSI

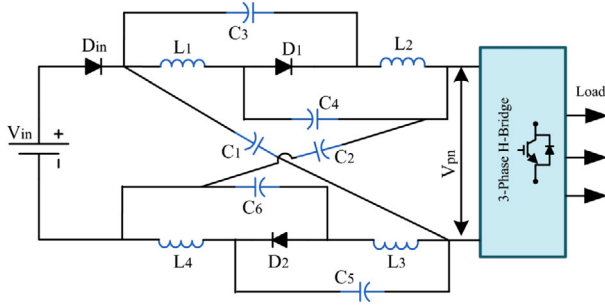


FIGURE 14 Basic modified capacitor-assisted ZSI (MCA-ZSI)

3.3 | Modified capacitor-assisted ZSIs (MCA-ZSIs)

A new switched capacitor-based complex ZSI structure, namely, a modified capacitor-assisted ZSI (MCA-ZSI), as shown in Figure 14, was studied in [72, 73] where two more extra capacitors (C_5 and C_6) are used to improve the boost factor of the topology. Although the MCA-ZSI provides very high voltage gain, the voltage stresses V_{C1} and V_{C2} across the main capacitors C_1 and C_2 are still very high compared to the traditional ZSI. Furthermore, the inrush current cannot be suppressed in this topology and there is no shared ground between the source and inverter bridge. To resolve these issues by maintaining such high gain, two new modifications [see Figure 15(a) and (b)] are brought out in [74, 75]. In [74], by making the entire Z network connection into series, the voltage stress across the capacitors is significantly reduced, and in addition to that, the start-up inrush current is also minimized as compared to the topology in [73]. Another additional advantage is the joint ground sharing which is absent in all modifications of the MCA-ZSI. On the other hand, in [75] [see Figure 15(b)], the input current is made continuous by applying embedded DC sources while keeping all features as unchanged. Later on, a set of two embedded switched capacitor-inductor ZSI (ECSL-ZSI) and reduced peak input current ECSL-ZSI (rECSL-ZSI) [76] came into existence [see Figure 15(c) and (d)] with improved outcomes in their configurations. Both ECSL-ZSI and rECSL-ZSI have adjusted the capacitor voltage stress and maintained the same high boost factor to that of a basic MCA-ZSI but the rECSL-ZSI possesses more superiority in terms of reducing peak and ripple of the input current of the inverter. However, passive components, i.e. capacitors on the impedance network of all capacitor-assisted ZSIs are more that increase the inverter cost and, thereby, decrease the efficiency.

3.4 | Embedded SL quasi ZSIs (ESL-qZSIs)

The conventional SL-qZSI has been redefined in [77] by merging ideas of both embedded and quasi ZSI structures. Hence, from the structural point of view, these inverters are termed as embedded SL quasi ZSI (ESL-qZSIs) [see Figure 16(a) and (b)]. The DC sources are placed in different positions

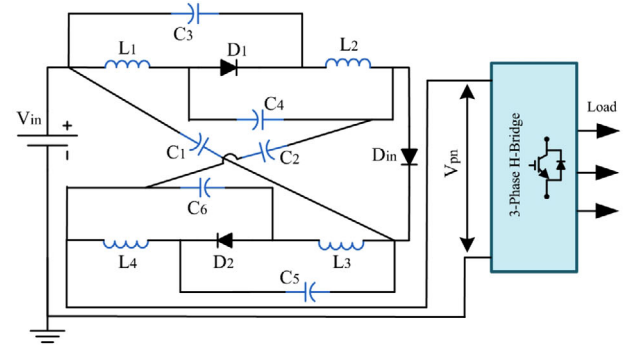


FIGURE 15 Different MCA-ZSI topologies

(a) SMCA-ZSI, (b) ESC-ZSI, (c) ECSL-ZSI, (d) rECSL-ZSI

inside the SL cells and the input current is made continuous with less amount of ripples. Here, the base frame is on the quasi structure; as a result, both ESL-qZSI and improved ESL-qZSI (iESL-qZSI) possess all inbuilt features of qZSI during the high-voltage boost operation. In [78], two structures, namely, modified enhanced-boost embedded switched-inductor

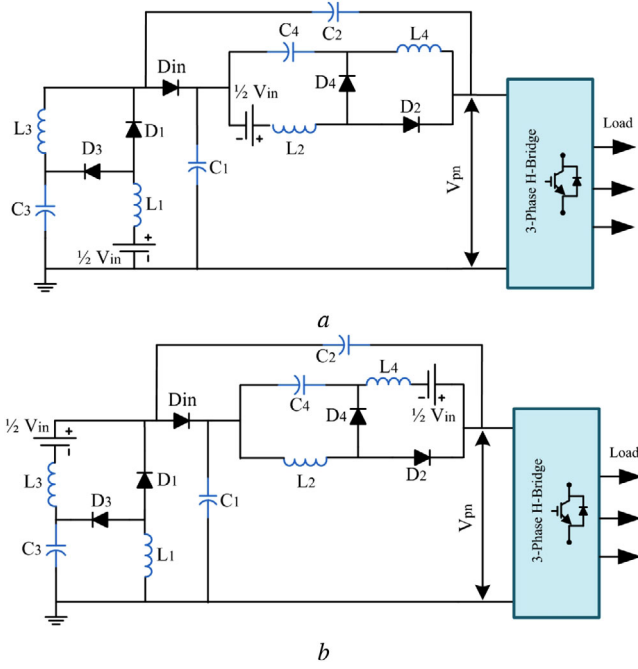


FIGURE 16 Different embedded SL quasi ZSI (ESL-qZSI) topologies
(a) ESL-qZSI, (b) iESL-qZSI

quasi-ZSI (MESL-qZSI) and improved modified enhanced-boost embedded switched-inductor quasi-ZSI (iMESL-qZSI) [see Figure 17(a) and (b)], have been investigated by following the structure in [77]. The boost factor of these inverters has been slightly stepped up by adding an additional capacitor in the impedance network. However, the number of diodes used is less than that of in [68]. Both designs have provided the parallel solution to overcome common issues. Furthermore, in [79], a combination of switched inductor-capacitor is employed to enhance the boost factor (see Figure 18) but the increased number of passive components, i.e. capacitors made the structure less enthusiastic compared to that presented in [77, 78].

3.5 | Similar structures

In the race of improving the voltage boost ability of the SL-ZSI, several other topologies have been studied in [80–84]. Most of these topologies follow the extended SL cell structures to improve the gain of the inverter. In [84], the model of an SL strong boost ZSI (SLSB-ZSI) (see Figure 19) was proposed where the SL cells have been composed on the multiple series impedance networks based on the idea in [85]. Although the SLSB-ZSI has significantly improved the boost factor and achieved lower voltage stress on capacitors and semiconductor switches, the component count is high enough that shrunk the practical applicability of the inverter. Other extensible switched ZSI topologies are configured in such a way that

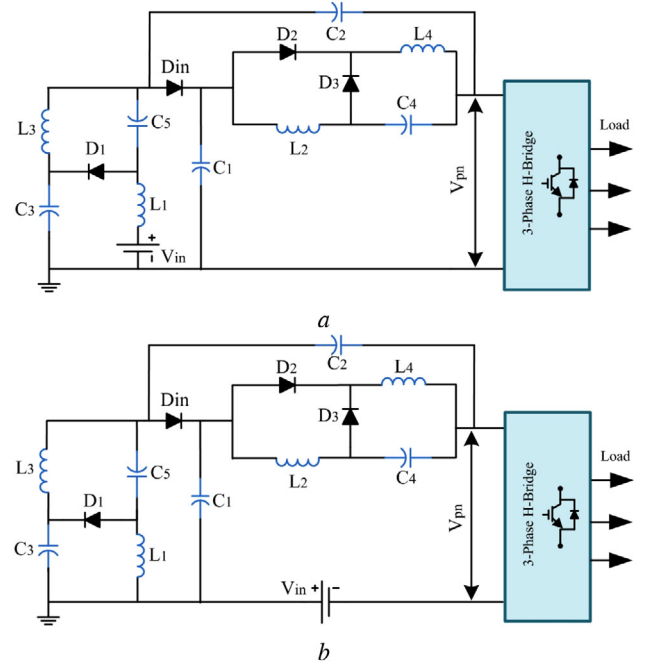


FIGURE 17 Different modified enhanced boost embedded SL quasi ZSI (MESL-qZSI) topologies
(a) MESL-qZSI, (b) iMESL-qZSI

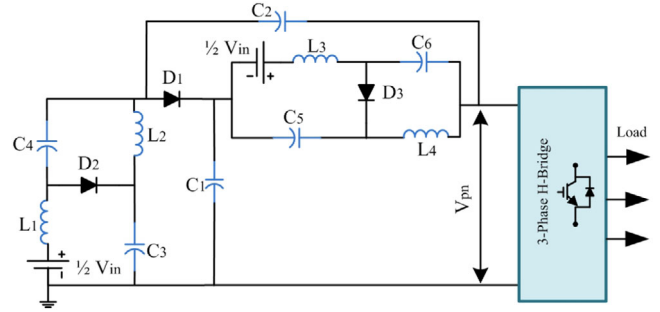


FIGURE 18 SIC-qZSI topology

several SL/SC cells can be added to improve the boost factor based on the requirement. All these topologies fall under the category of quasi and embedded ZSIs having the same conventional feature with the elevated boost factor. Tables 4 and 5 summarize the key features of the basic SL-based ZSI models and primarily designed two symmetric Z-impedance switched ZSI topologies, respectively. Furthermore, the common structural characteristics of different switched ZSIs are highlighted in Table 6.

3.6 | Results and structural analysis of ZSIs

The simulation study of the recently developed SL/SC-based ZSI topologies has been carried out by adopting the impedance network parameters from [63] as shown in Table 1. Mainly, four

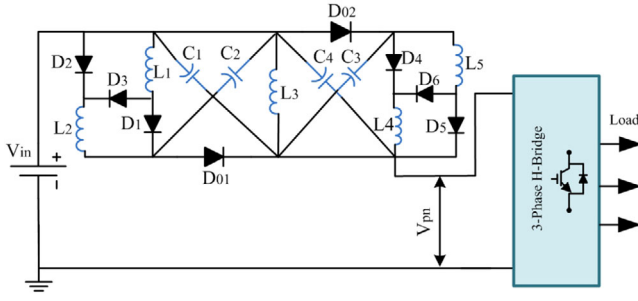


FIGURE 19 SLSB-ZSI topology

TABLE 1 Simulation parameters

No.	Parameters	Value
1	Input voltage, V_{in}	50 V
2	Inductors, L	700 μ H
3	Capacitors, C	500 μ F
4	Three-phase load, R_L	60 Ω and 5 mH
5	Switching frequency, f_s	10 kHz
6	Modulation index, M and duty shoot-through, D_s	0.8 and 0.2

most significant topologies such as EB-ZSI [63], EB-qZSI [68], MCA-ZSI [73], and ESL-qZSI [77] are considered in this study. The DC-link voltage (V_{pn}) of the inverter which represents the inverter boost factor (B) by expressing the ratio of the input DC voltage to the generated DC-link voltage, i.e. $B = V_{pn}/V_{in}$, is one of the most important concerns. The voltage gain comparison can be carried out by finding the DC-link voltage of any ZSIs. As boost factor is one of the most common improvements that is claimed in the literature, this study has taken it as the prime feature. On the other hand, the two most prevailed drawbacks such as the induced voltage stress on capacitors and inrush current generation at the beginning of operation are taken as the second and third important features, respectively. All these three features spontaneously express the behaviour and performance of any designed ZSIs. In this study, the input DC voltage (V_{in}), ST duty ratio (D_s), and modulation index (M) are taken as 50 V, 0.2, and 0.8, respectively, in order to generate consistent outcomes. From the simulation, the obtained results are shown in Figures 20–23 for [63], [68], [73], and [77], respectively. According to the simulation results, it can be seen that the DC-link voltage is same for all three [63], [68], and [77] which is 177 V for the input of 50 V while the value was found 250 V for the [73]. It is a clear understanding that [73] has the highest voltage boost ability than all for the same input and duty ratio. Regarding the capacitor voltage during the boost operation, [63] and [73] could not show the satisfactory performance compared to [68] and [77]. However, [73] has reduced the stress across the capacitors ($C_3 - C_6$) which are used outside of the main X-shape of the MCA-ZSI network. For [68] and [77], almost all capacitors used in the impedance network have a low voltage impression on them, which is one of the most important outcomes of these two topologies. The values

TABLE 2 Results summary

Ref.	DC-link voltage	Capacitor voltage	Input current
[63]	177 V	141.9 V 113.7 V	3×10^4 A
[68]	177 V	113 V, 28 V 78 V, 64 V	165 A
[73]	250 V	150 V 50 V	3×10^4 A
[77]	177 V	88.72 V 53.31 V	168 A

of the generated voltage for different capacitors can be seen in Figures 21(b) and 23(b) for [68] and [77], respectively. The third and the last feature is the input current behaviour while starting up. From Figures 20(c) and 21(c), the inverters in [63] and [73] have no input current suppression ability during the start-up and the value is very high and severe; thus, these impose transient current stress on the circuit. In contrast, the results for [68] and [77] as shown in Figures 21(c) and 23(c), respectively, have significantly reduced the input current spike compared to [63] and [73]. The values of all four input currents can be seen in Figures 20(c)–23(c). Although topologies in [68] and [77] have shown the inrush current suppression ability, the magnitudes of the start-up current (i.e. 165 and 168 A, respectively) are still high. Note that these high current amplitudes depend on the value of inductors and capacitors in the impedance network and the resonance frequency they form. For better comparison, all these values are provided in Table 2. The results obtained from the simulation have maintained the in-line relation with the theoretical claims of those studies. Based on the results and analysis, the following points can be noted:

1. The quasi and embedded-quasi SL-ZSI structures have less voltage and current stress in the overall inverter network.
2. The shared common ground in quasi and embedded-quasi structures helps to significantly reduce the inrush current suppression as well as the component voltage stress.
3. The overall size, weight, and cost are less for quasi and embedded-quasi structures.

The characteristics curve to analyze the boost factor with respect to ST duty cycle is shown in Figure 24. All basic SL-ZSI topologies are compared along with these four SL/SC-based ZSI topologies to show the overall behaviour within their duty cycle range. From Figure 24, it can be seen that the MCA-ZSI and ECSL-ZSI [76] have the highest boost factor in their entire duty cycle control region compared to all other ZSIs. Another important observation is that the boost factor curve for all three basic topologies such as SL-ZSI [30], SL-EZSI [34], and SL-IZSI [35] exist below the region of recently developed two switched impedance network-based EB-ZSI [63], EB-qZSI [68], ESL-qZSI [77], and MCA-ZSI [73] topologies. Although all these two switched network topologies have used more capacitors for attaining high boost effect, the induced voltage stress is

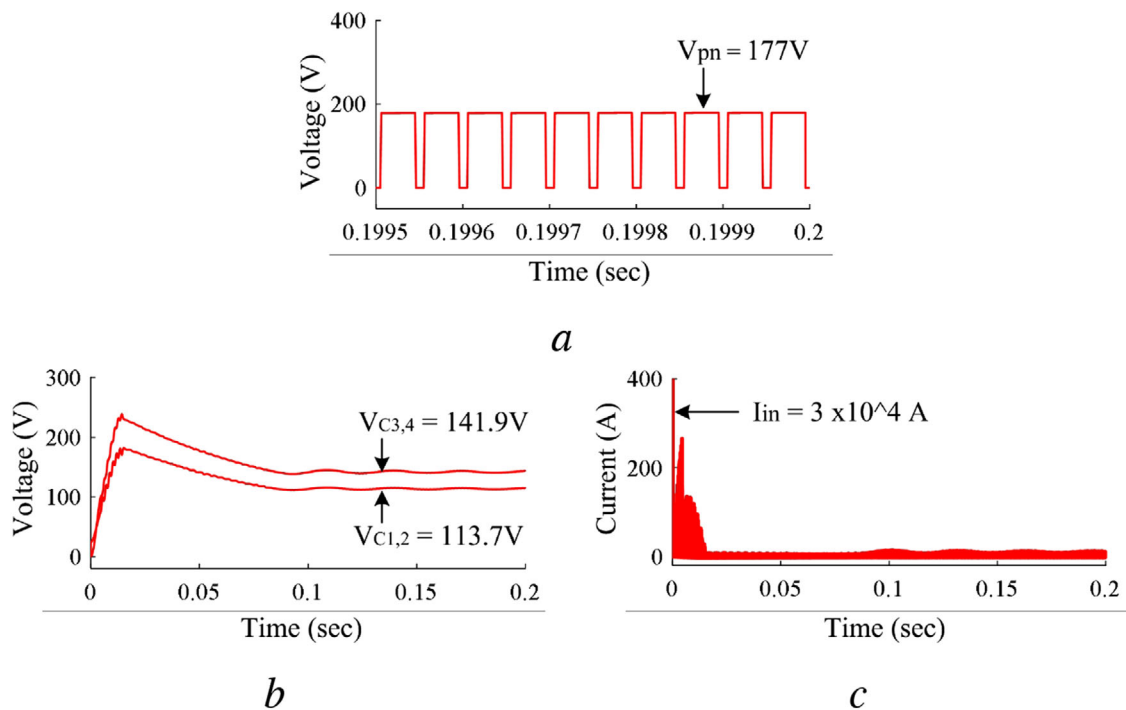


FIGURE 20 Simulation results of EB-ZSI

(a) DC-link voltage, V_{pn} , (b) capacitor voltages, $V_{C1,2}$ and $V_{C3,4}$, (c) input current, I_{in}

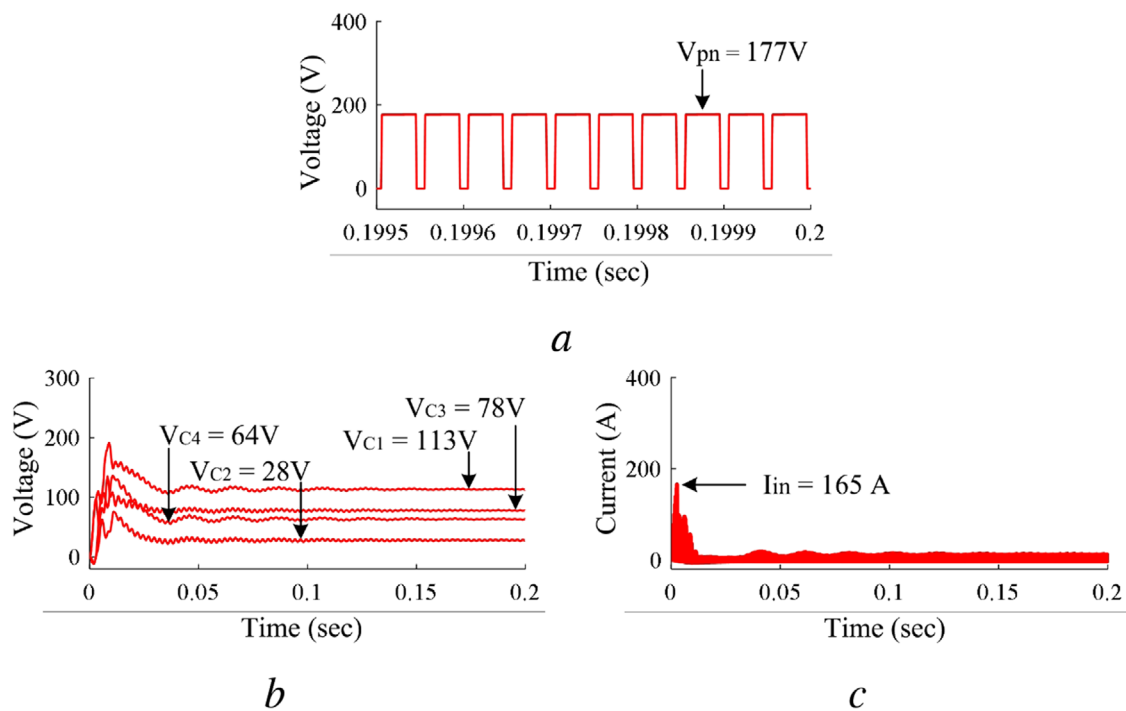


FIGURE 21 Simulation results of EB-qZSI

(a) DC-link voltage, V_{pn} , (b) capacitor voltages, V_{C1} , V_{C2} , V_{C3} , and V_{C4} , (c) input current, I_{in}

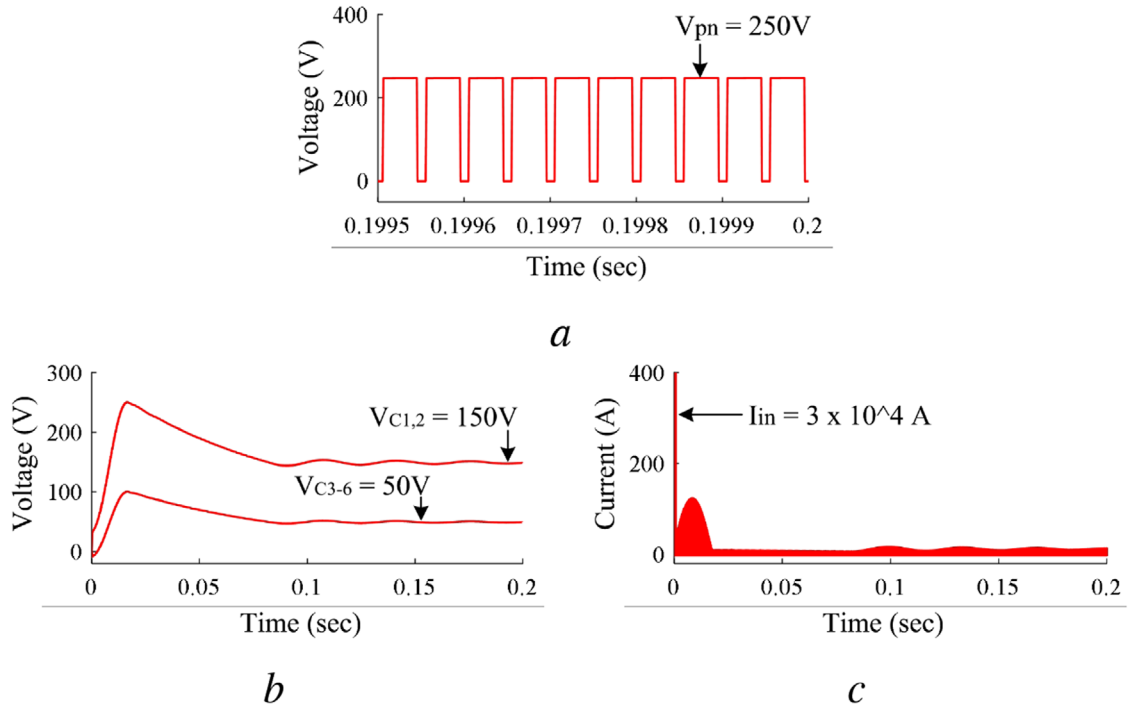


FIGURE 22 Simulation results of MCA-ZSI

(a) DC-link voltage, V_{pn} , (b) capacitor voltages, $V_{C1,2}$, and V_{C3-6} , (c) input current, I_{in}

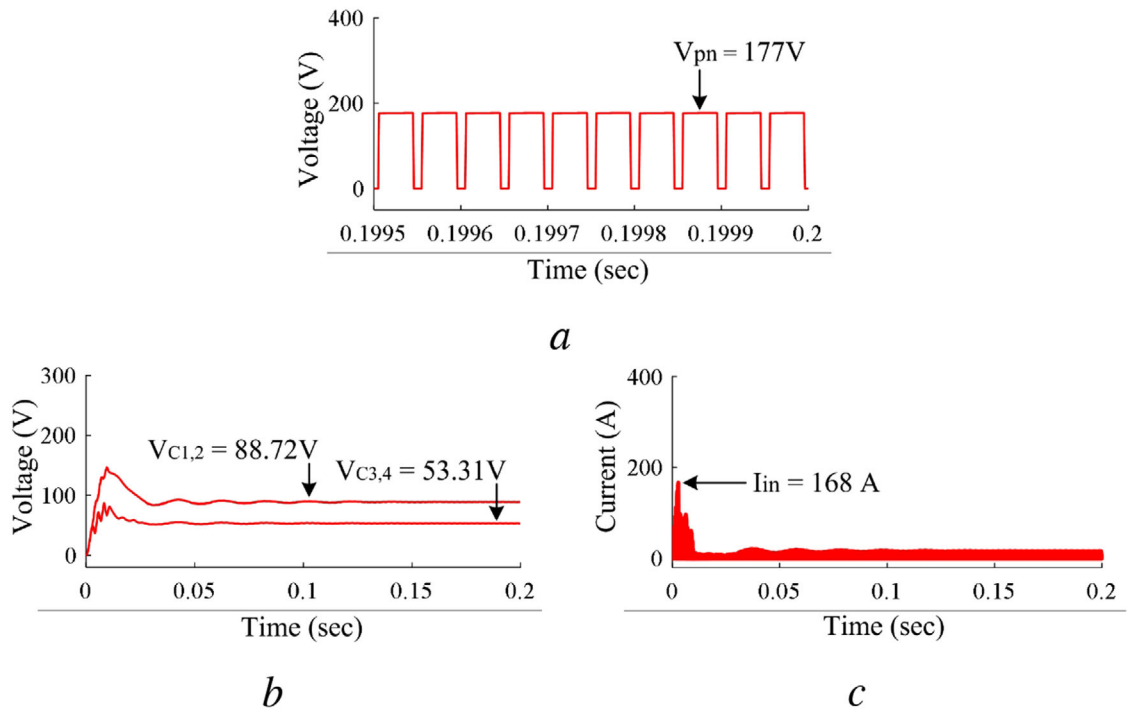


FIGURE 23 Simulation results of ESL-qZSI

(a) DC-link voltage, V_{pn} , (b) capacitor voltages, $V_{C1,2}$ and $V_{C3,4}$, (c) input current, I_{in}

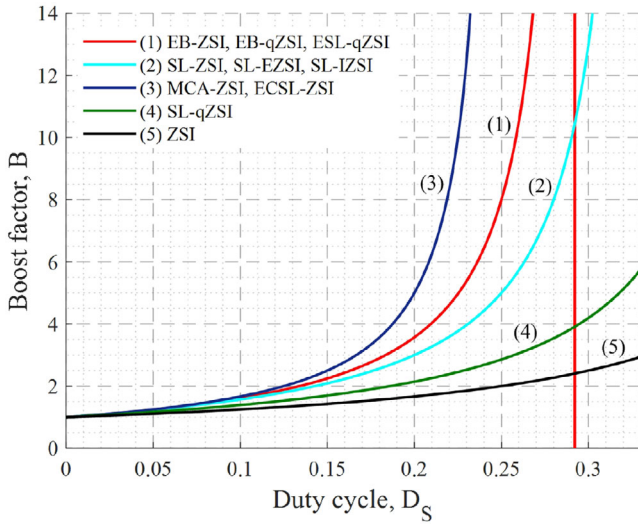


FIGURE 24 Boost factor comparison of SL-ZSI topologies

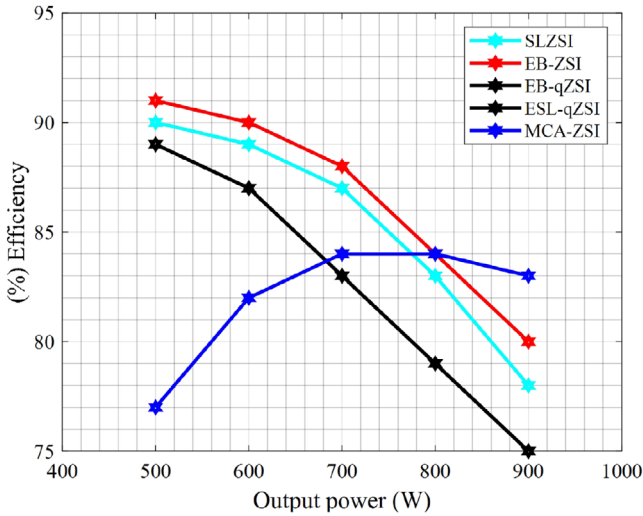


FIGURE 25 Efficiency comparison of SL/SC-ZSI topologies

distributed on the capacitors and, hence, the requirement and size of capacitor become low compared to conventional SL-ZSIs. Thus, the objective of simultaneously elevating the voltage boost and reducing the voltage stress has satisfactorily met.

Figure 25 shows the efficiency comparison of SL/SC-based ZSI topologies along with basic SL-ZSI structure. According to the parameters in [68] which are also provided in Table 3, the efficiencies of the converters are analyzed. The SBC modulation control technique as mentioned before has been applied

TABLE 3 Efficiency calculation parameters [68]

ESR of inductor (r_L)	ESR of capacitor (r_C)	Diode forward voltage drop, (v_L)	MOSFET RDS(on)
92 m Ω	120 m Ω	1.3 V	0.27 Ω

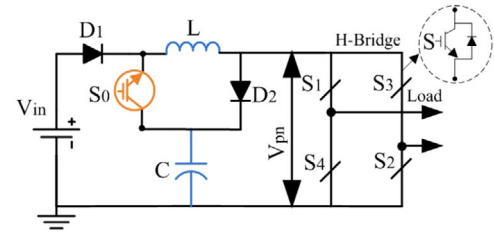


FIGURE 26 Classical switched boost inverter (SBI)

for all converter topologies. The parametric values of components such as the equivalent series resistance (ESR) of the inductor, ESR of the capacitor, forward voltage drop of the diode, and semiconductor switch on state drain-source resistance have impacts on the converter efficiency. In this study, for generating the same boost factor of 3.57 with the DC input of 50 V, the ST duty ratio is varied for these converters. From Figure 25, it can be seen that EB-ZSI in [63] has higher efficiency compared to all other converters. The efficiency outcomes of the EB-qZSI [68] and ESL-qZSI [77] are identical as well as stay below the region of [63] despite the same components count. On the other hand, having more passive components in the structure, the MCA-ZSI [73] shows the lowest efficiency at starting whereas it hits the peak efficiency at 700 W and performs well until 900 W. The efficiency curve of the SL-ZSI [30] topology lies under the region of topologies [63], [68], and [77] which gives a closer outcome to that of [63] for the entire region. Moreover, the practical implementation of these converters can ensure the accurate efficiency during their operation. Note that the efficiency outcome of any individual converter may vary depending on the parametric value of the components. Hence, efficiencies of all these converters can be improved by means of appropriate design and selection of parameters.

4 | TOPOLOGY IMPROVEMENTS OF SWITCHED BOOST ZSI

The typical application of impedance source converters is the power grid and microgrid where the ZSI can serve as a reliable power conditioning system (PCS). However, in the DC nanogrid, which is a renewable energy based common DC distribution system for residential load demands; the size, weight, and cost of PCS play a crucial role. Hence, the classical ZSIs may not be a suitable option for such kind of application. A simple structure with less component in the LC network, known as SBI was introduced in [86], which ideally falls in the category of impedance source inverter. Figure 26 shows the structure of the basic SBI topology. The idea of SBI was developed based on the inverse Watkins–Johnson topology [87, 88] which is best suited for the low-power application. The control technique of a classical SBI was studied in [89, 90]. In [91, 92], the SBI was first used as a power electronic interface, i.e. PCS where, from a single DC input, it can simultaneously supply both DC and AC loads. The topological developments of the SBI are addressed in the following subsections where the several issues are solved

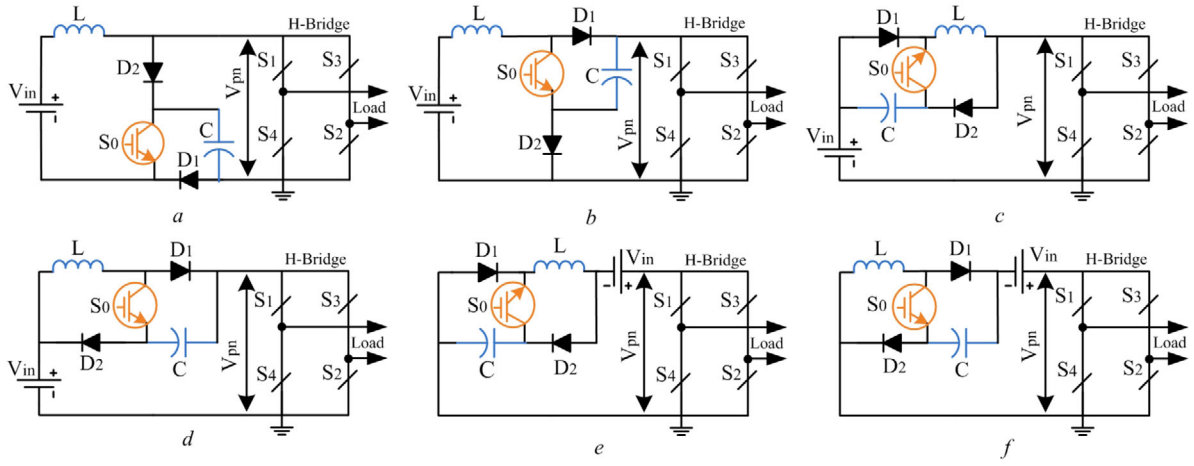


FIGURE 27 Different qSBI topologies

(a) qSBI-T1, (b) qSBI-T2, (c) negative bus-T1, (d) negative bus-T2, (e) positive bus-T1, (f) positive bus-T2

and significantly improved by different techniques and modifications.

4.1 | Basic switched boost inverter (SBI)

In Figure 26, the SBI impedance network consists of only one pair of LC components, i.e. the capacitor (C) and the inductor (L). In comparison to the classical ZSI, an additional diode (D) and active switch (S) have been utilized in the SBI structure. In this structure, the input and bridge network share the same ground. Moreover, the SBI exhibits better electromagnetic interference noise immunity as the ST takes place during the inverter control operation. The SBI possesses the same buck–boost feature as of the classical ZSI but the boost factor is only $(1 - D_S)$ times than the ZSI. Besides, the capacitor (C) is connected to the negative DC bus of the inverter bridge and exposed to high voltage stress as the inverter DC-link voltage (V_{pn}) is similar to the capacitor voltage (V_C) during the boost operation. As a result, the high capacitor voltage stress limits the freedom of high boost operation. Furthermore, the SBI draws a discontinuous input current which reduces the lifespan of sources [93].

By keeping all these problems in mind, a class of quasi SBIs (qSBIs) was studied in [94] and the comparison between the qZSI and qSBI was carried out in [96]. In [94], the inductor (L) is directly placed with the input DC source in the embedded-type qSBIs that draws continuous input current and boosts the DC bus voltage than traditional SBI [see Figure 27(a) and (b)]. The qSBI-T1 does not share common ground whereas the qSBI-T2 shares the ground between the input and output side of the converter. However, both of these two topologies could not reduce the high voltage stress on capacitors. Further modifications with two DC-link type topologies show less stress [see Figure 27(c)–(f)] by maintaining the basic properties

of qSBIs. In [97], a dual SBI (D-SBI) model is proposed where the boost factor is improved than the classical SBI but the component count is higher, even more than the ZSI. However, the D-SBI has given an idea of cascading SBI networks to achieve higher voltage gain from a low input voltage supply. Similarly, for electrochemical and electroplating application [98], a half-bridge ZSI network is used and based on that concept, various half-bridge SBIs (HB-SBIs) (see Figure 28) were studied in [99–103].

4.2 | SL/SC switched boost inverter (SC/SL-SBI)

The boost factor of all basic SBIs is still less than the classical ZSI and, hence, the SL technique was applied in [104]. Figure 29(a) and (b) shows two different configurations of a SL-SBI which are known as ripple input SL-SBI (rSL-SBI) and continuous input current SL-SBI (cSL-SBI), respectively. In both structures, one additional inductor and three diodes are utilized. In addition, an investigation of placing the DC source in different positions of the impedance network according to [105] was done. Although SL-SBIs have higher voltage gain, it has several demerits such as large voltage stress on diodes, switch, and capacitors. In [106], the basic SBI structure is reconfigured to an embedded structure termed as ESL-SBI by inserting the DC source (V_{in}) inside the impedance network. As a result, the input current becomes continuous. Furthermore, this model is configured with an SL cell in the network which is also extensible to n cells. The circuit configuration is exactly the same as shown in Figure 29(a). Unfortunately, neither [104] nor [106] is able to minimize the voltage stress on components despite the high voltage gain. In order to mitigate the common problems, a SC cell-based SBI known as (SC-SBI) (see Figure 30) was proposed in [107]. Using the less number of diodes and

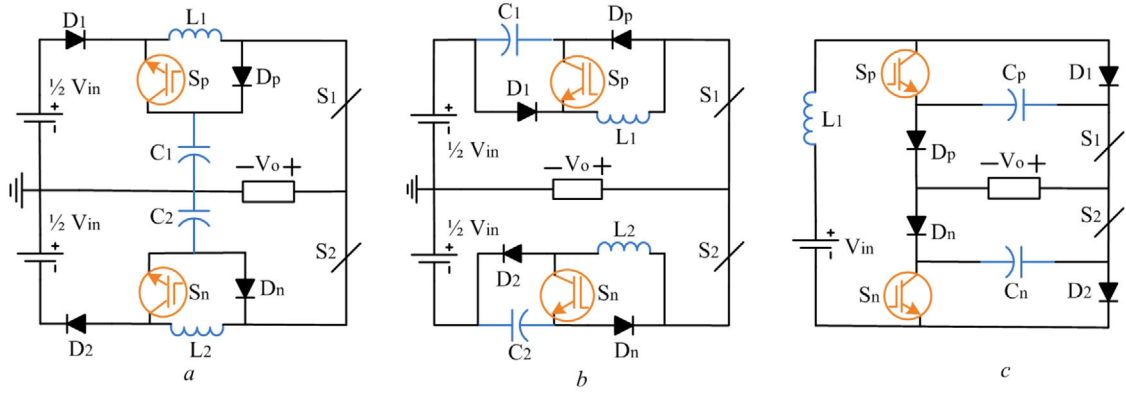


FIGURE 28 Different half-bridge SBI topologies

(a) HB-SBI, (b) HB-qSBI, (c) (CIC) HB-SBI

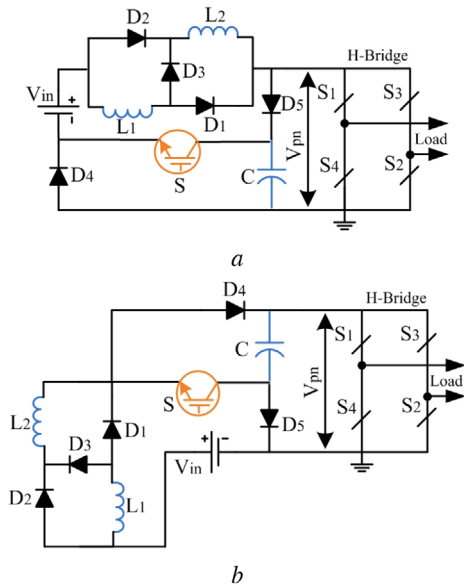


FIGURE 29 Switched inductor SBI topologies (SL-SBIs)

(a) rSL-SBI, (b) cSL-SBI

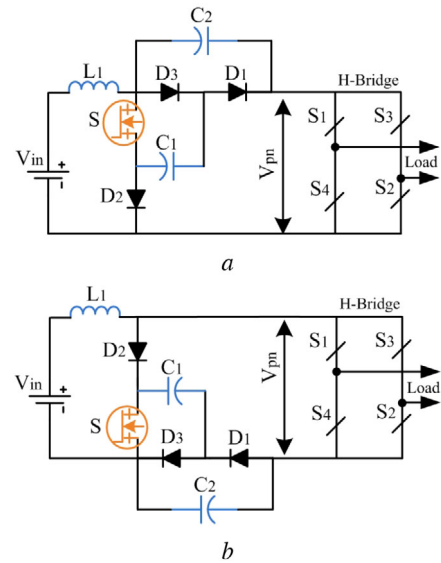


FIGURE 30 Switched capacitor qSBI topologies (SC-SBIs)

(a) SCq-SBI-T1, (b) SCq-SBI-T2

inductors, the converter in [107] generates more voltage boost than that of in [104] and [106]. Furthermore, the SC-SBI has several advantages like improved input and ST current profile along with reduced voltage stress on diodes, switches, and capacitors.

4.3 | High gain and enhanced boost SBI

To keep pace with the trend, several high-voltage gain SBI topologies were studied in [108–110]. Figure 31(a) and (b) represents two quasi-SBI topologies where the impedance network uses less active components, i.e. diodes compared to SL/SC-

SBIs but produces more voltage boost by placing inductor (L_2) and capacitor (C_2) into the embedded-type qSBIs. Having the same component, [110] can produce the boost effect similar to that as presented in [109]. It can be noted that all of these high-gain SBIs have high voltage stress on the additional switch, capacitor, and diodes, which is exactly the same as their DC-link voltages. In [111, 112], two quasi network-based SBI models as shown in Figure 32 are designed with an additional diode and capacitor comparing that in [108]. Compared to the topology in [112, 111] has enhanced the overall performance. Bearing in mind, all of these ideas are parallel attempts and some of them came one after another to improve existing models. An active switch-enhanced boost q-SBI (EB-qSBI) as shown in Figure 33(a) and presented in [113] has omitted two inductors

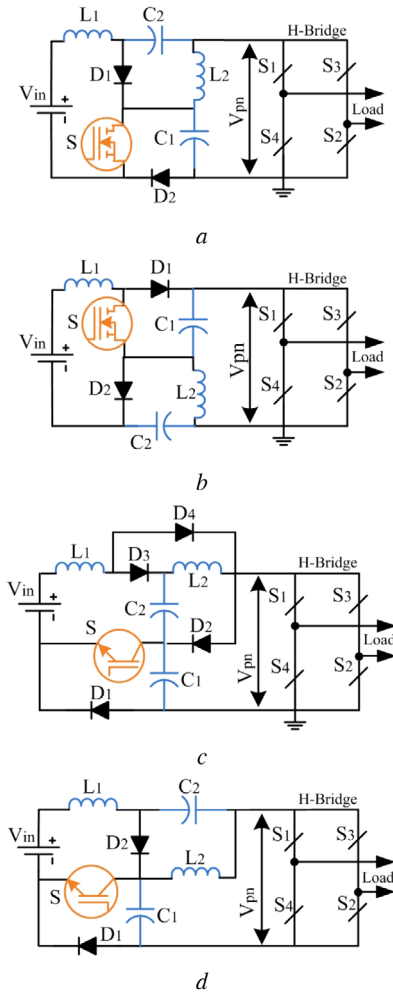


FIGURE 31 Different high gain switched SBI topologies

(a) HG-qSBI-T1, (b) HG-qSBI-T-2, (c) HG-SBI, (d) HS-SZSI

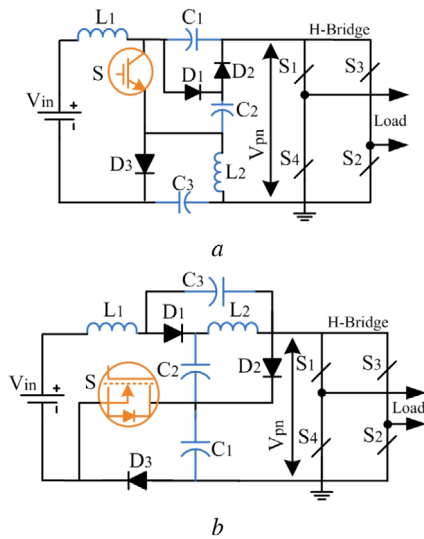


FIGURE 32 Different high voltage gain qSBI topologies

(a) HG-qSBI, (b) S-qSBI

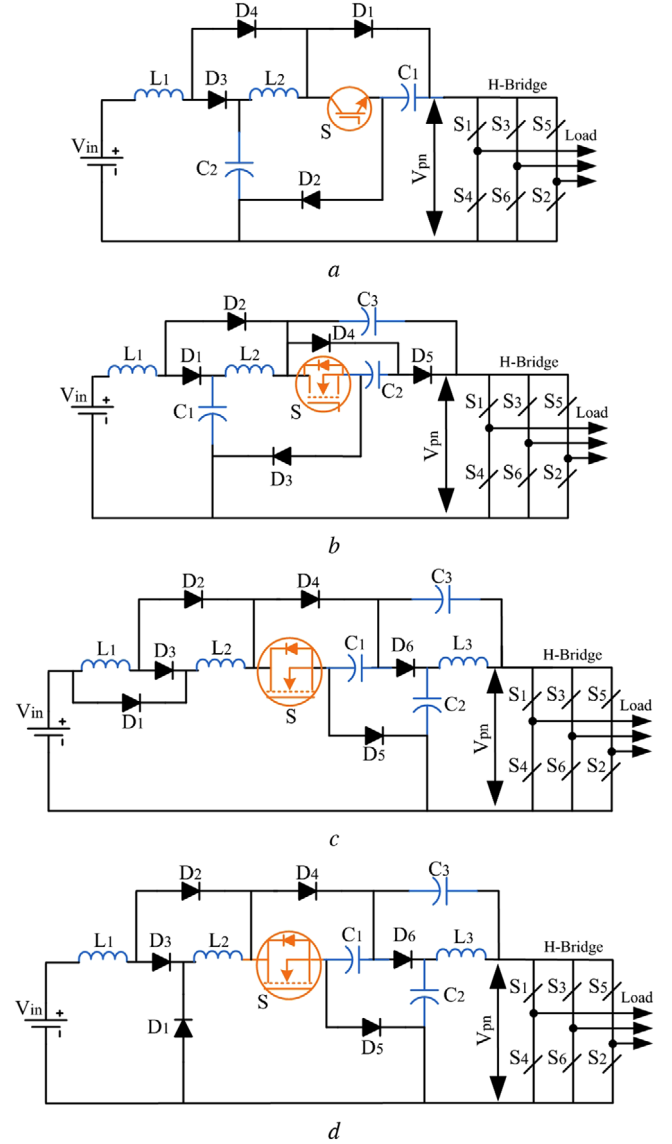


FIGURE 33 Different enhanced boost active switch ZSI topologies

(a) EB-qSBI, (b) EB-qSBI 2019, (c) rASLB-qZSI, (d) cASLB-qZSI

and two capacitors and replaced one diode with an active switch. The current stress of the switch is reduced which in turn reduces the conduction losses of the switch and improves inverter's efficiency. In addition, the EB-qSBI shares common ground and draws continuous input current. In [114], similar network [see Figure 33(b)] has been extended with one more additional diode and capacitor for further gain enhancement. If we look at [115], two other models consisting a large number of active and passive devices have slightly improved the boost factor than that of in [113] [see Figure 33(c) and (d)]. These topologies are termed as ripple input current active SL boost qSBI (rASLB-qSBI) and continuous input current active SL boost qSBI (cASLB-qSBI), respectively. Both of these cannot suppress the voltage stress on components during the boosting operation, which restricts their performance in high voltage gain applications.

TABLE 4 Summary of different basic SL-ZSI topologies

Ref.	Topology	Boost factor	No. of inductor (L) and capacitor (C)	No. of diode (D) and DC source (V _{in})	Features
[30]	SL-ZSI	$\frac{(1+D_S)}{(1-3D_S)}$	L = 4 & C = 2	D = 7 & V _{in} = 1	- High boost factor - Discontinuous input current - Higher capacitor voltage stress and start-up inrush current
[33]	SL-qZSI	$\frac{(1+D_S)}{(1-2D_S-D^2)}$	L = 3 & C = 2	D = 4 & V _{in} = 1	- Continuous input current - Reduces the voltage stress on C ₂ - Common ground facility - Low boost factor
[34]	SL-EZSI	$\frac{(1+D_S)}{(1-3D_S)}$	L = 3 & C = 2	D = 7 & V _{in} = 2	- Inherent ability of input current filtering - Lower blocking voltage diode - Requires two input DC sources
[48]	rSL-qZSIcSL-qZSI	$\frac{(1+D_S)}{(1-3D_S)} \frac{1}{(1-3D_S)}$	L = 3 & C = 2	D = 7 & V _{in} = 1	- Reduces active and passive component sizing - Continuous input current with less input ripple - Inrush current suppression ability
[52]	rESL-ZSIcESL-ZSI	$\frac{(1+D_S)}{(1-3D_S)} \frac{1}{(1-3D_S)}$	L = 3 & C = 2	D = 7 & V _{in} = 2	- Draws smooth filter-less DC current - Less voltage stress on components - Continuous input current - Two DC sources required
[35]	SL-IZSI	$\frac{(1+D_S)}{(1-3D_S)}$	L = 3 & C = 2	D = 7 & V _{in} = 1	- Inrush current suppression ability - Reduces voltage stress on capacitors - Discontinuous input current

4.4 | Active switch SC/SL boost SBI

The SBIs with active switches have been expanded to SC/SL-based SBIs in [116–121]. All these topologies have particularly used a quasi or embedded ZSI skeleton and appeared as SBIs. Various structures of such SBIs can be seen in Figure 34 where the configurations as shown in Figure 34(a) and (b) have improved the voltage gain capability by adopting the SC-SL cells inside the impedance network. The initial SBI and qSBI models with SC/SL cells including an active switch represent the SC/SL SBI (i.e. ASC/SL-SBI) [116] and an active SC/SL qSBI (i.e. ASC/SL-qSBI) [117], respectively. The main motivation for developing these inverters came from the same drawbacks that are unveiled in the prior literature. From Figure 34(c) and (d), it can be observed that the gain has further been extended in [119] and [121] by adding an additional LC pair in the network and termed as extended active-switched qSBI (EAS-qSBI) and extended boosting switched-capacitor embedded qSBI (ESCE-qSBI), respectively. In [122–124], a continuous current mode SBI network was studied, and later, the topology in [125] used an SL cell inside the impedance network in order to maximize the inverter gain. Figure 35(a) shows the modified SBI (M-SBI) while Figure 35(b) and (c) shows the SL-modified qSBI (SLM-qSBI) and hybrid switched-inductor-capacitor modified qSBI (HSLCM-qZSI), respectively. The off-

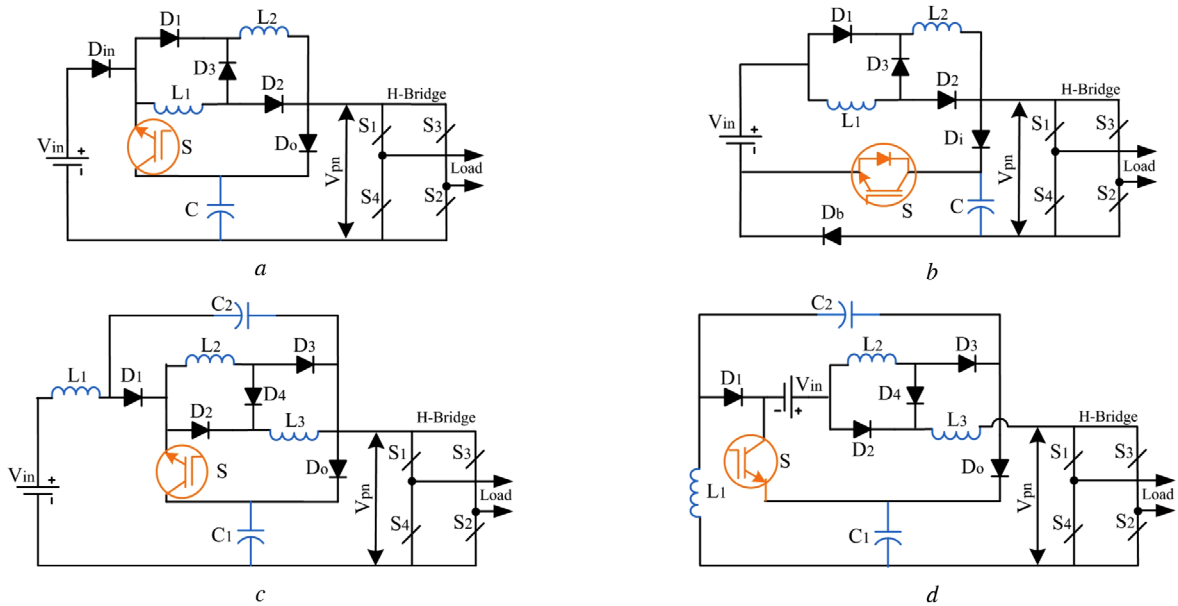
spring modifications can be found in [122, 126] pertaining to the structures. Some other similar models as shown in Figure 36 were presented in [127, 128], where Figure 36(a) and (b) represents SLC-SBI-T1 and SLC-SBI-T2 inverters, respectively. At the same time, an enhanced SLC-SBI (eSLC-SBI) is shown in Figure 36(c). All of these inverters have strong voltage inversion ability but the number of active component count is high that increases losses and, ultimately, reduces the efficiency of the inverter. The summary of all these predominant SBI topologies is presented in Table 7 whereas the boost factor comparison of all recently developed SBIs is shown in Figure 37. The boost factor of all primary SL/SC-based SBI topologies is considered and compared with respect to the same ST duty cycle. The behaviour of the inverter voltage boost ability with respect to the changes in the duty ratio can be understood from these curves. From Figure 37, it can be seen that the recently developed SL/SC-based SBI topologies have improved their boost factors in the whole duty range as compared to the classical SBI and qSBI topologies. Figure 38 shows the efficiency curves of several SBI topologies with their respective parametric values. The data are taken from the qSBI [90], SL-qSBI and SC-qSBI [107], HG-SBI and HG-qSBI [108], EB-qSBI [113], EB-qSBI2 [114], rASLB-qSBI [115], and M-SBI [123] to plot the efficiency curves. From Figure 38(a), it can be observed that the qSBI has a fair and nearly-steady efficiency outcome in the

TABLE 5 Summary of two symmetric Z-network-based ZSI topologies

Ref.	Topology	Boost factor	No. of Inductor (L) and Capacitor (C)	No. of Diode (D) and DC source (V _{in})	Features
[63]	EB-ZSI	$\frac{1}{(1-4D_3+2D_3^2)}$	L = 4 & C = 4	D = 5 & V _{in} = 1	- Combined two Z networks - Higher modulation index improves output waveform - Current and voltage stress can not be suppressed
[68]	EB-qZSI	$\frac{1}{(1-4D_3+2D_3^2)}$	L = 4 & C = 4	D = 5 & V _{in} = 1	- Low shoot-through driven inverter - Possess all features of quasi network - Cost effective design
[73]	MCA-ZSI	$\frac{(1-D_3)}{(1-5D_3+4D_3^2)}$	L = 4 & C = 6	D = 3 & V _{in} = 1	- Very high boost factor - Bulky size and high cost - Huge inrush current and capacitor voltage stress
[77]	ESL-qZSI	$\frac{1}{(1-4D_3+2D_3^2)}$	L = 4 & C = 4	D = 5 & V _{in} = 2	- Low ripple and continuous input current - Lower component voltage stress - Reduces capacitor sizing
[84]	SL-SBZSI	$\frac{(2-3D_3-5D_3^2)}{2(1-7D_3+12D_3^2)}$	L = 5 & C = 4	D = 8 & V _{in} = 1	- Strong voltage boost ability - Lower inrush current - High component counts and cost
[79]	SIC-qZSI	$\frac{1}{(1-4D_3)}$	L = 4 & C = 6	D = 3 & V _{in} = 2	- High boost factor - Lower input and inductor current - High passive component count

TABLE 6 Characteristics of different SL-ZSI topologies

Parameters	[30]	[33]	[34]	[48]	[52]	[35]	[63]	[68]	[73]	[77]	[76]	[84]	[79]
Impedance network type	SL	SL	SL	SL	SL	SL	SL-SC	SL-SC	SC	SL	SL-SC	SL	SL-SC
Inrush current	✓	×	×	×	×	×	✓	×	✓	×	×	×	×
Continuous input current	×	✓	✓	✓	✓	×	✓	×	×	✓	✓	×	✓
Common ground	×	✓	×	✓	×	✓	×	✓	×	✓	×	✓	✓

**FIGURE 34** Active switched ZSI topologies

(a) ASCSL-SBI, (b) ASCSLq-SBI, (c) EASq-SBI, (d) ESCEq-SBI

TABLE 7 Summary of SBI Topologies

Ref.	Topology	Boost factor	No. of (L) and (C)	No. of (D) and switch (S)
[86]	SBI	$\frac{(1-D_S)}{(1-2D_S)}$	L = 1 & C = 1	D = 2 & S = 1
[94]	qSBI-T1qSBI-T2	$\frac{1}{(1-2D_S)} \frac{(1-D_S)}{(1-2D_S)}$	L = 1 & C = 1	D = 2 & S = 1
[100]	HB-SBI	$\frac{(1-D_S)}{2(1-3D_S)}$	L = 2 & C = 2	D = 4 & S = 2
[102]	HB-qSBI	$\frac{(1-D_S)}{2(1-3D_S)}$	L = 2 & C = 2	D = 4 & S = 2
[104]	cSLBIrSLBI	$\frac{(1+D_S)}{(1-3D_S)} \frac{1}{(1-3D_S)}$	L = 2 & C = 1	D = 5 & S = 1
[107]	SC-qSBI	$\frac{2}{(1-2D_S)}$	L = 1 & C = 2	D = 3 & S = 1
[108]	HG-qSBI	$\frac{1}{(1-4D_S+2D_S^2)}$	L = 2 & C = 2	D = 2 & S = 1
[109]	HG-SBI	$\frac{1}{(1-3D_S+D_S^2)}$	L = 2 & C = 2	D = 4 & S = 1
[110]	HS-SBI	$\frac{1}{(1-3D_S+D_S^2)}$	L = 2 & C = 2	D = 2 & S = 1
[111]	HG-qSBI	$\frac{(2-D_S)}{(1-3D_S+D_S^2)}$	L = 2 & C = 3	D = 3 & S = 1
[112]	S-qSBI	$\frac{1}{(1-3D_S)}$	L = 2 & C = 3	D = 3 & S = 1
[106]	ESL-SBI	$\frac{(1+D_S)}{(1-3D_S)}$	L = 2 & C = 1	D = 5 & S = 1
[113]	EBqS-SBI	$\frac{1}{(1-4D_S+2D_S^2)}$	L = 2 & C = 2	D = 4 & S = 1
[115]	rASLB-qSBICASLB-qSBI	$\frac{1}{(1-4D_S+D_S^2)} \frac{1}{(1-4D_S+D_S^2)}$	L = 3 & C = 3	D = 6 & S = 1
[116]	ASC/SL-SBI	$\frac{(1-D_S)}{(1-3D_S)}$	L = 2 & C = 1	D = 5 & S = 1
[118]	ASC/SL-qSBI	$\frac{(1+D_S)}{(1-3D_S)}$	L = 2 & C = 1	D = 5 & S = 1
[119]	EAS-qSBI	$\frac{(1-D_S)}{(1-4D_S+D_S^2)}$	L = 3 & C = 2	D = 5 & S = 1
[121]	ESC-EqSBI	$\frac{(1+D_S)}{(1-4D_S+D_S^2)}$	L = 3 & C = 2	D = 5 & S = 1
[123]	M-SBI	$\frac{1}{(1-3D_S+D_S^2)}$	L = 2 & C = 2	D = 2 & S = 1
[125]	SLM-qSBI	$\frac{(1+D_S)}{(1-3D_S)}$	L = 3 & C = 2	D = 5 & S = 1
[125]	HSLCM-qSBI	$\frac{1}{(1-4D_S+2D_S^2)}$	L = 3 & C = 4	D = 3 & S = 1
[127]	SLC-SBI-T1	$\frac{(1+D_S)}{(1-3D_S)}$	L = 2 & C = 1	D = 4 & S = 2
[127]	SLC-SBI-T2	$\frac{1}{(1-4D_S+2D_S^2)}$	L = 2 & C = 2	D = 3 & S = 2
[128]	eSLC-SBI	$\frac{2}{(1-4D_S+2D_S^2)}$	L = 2 & C = 3	D = 5 & S = 1

whole power delivery range. In Figure 38(b) and (c), it is clearly shown that the SC-qSBI has better efficiency outcome than the SL-qSBI having the same parameters. Similarly, looking at Figure 38(d) and (e), it can be found that the HG-qSBI has a superior performance than the HG-SBI. In Figure 38(f)–(h), the efficiency curves of the EB-qSBI, EB-qSBI2, and rASLB-qSBI are shown, where, despite more number of components than the EB-qSBI, both EB-qSBI2 and rASLB-qSBI topologies maintain an upright trend in the efficiency outcome with nearly the same parameters. Finally, in Figure 38(i), the M-SBI shows a competent efficiency with given parameters. From all these efficiency outcomes, the suitable SBI topology can be easily identified for the targeted application. The following section provides a concise outlook about the current challenges and future research directions.

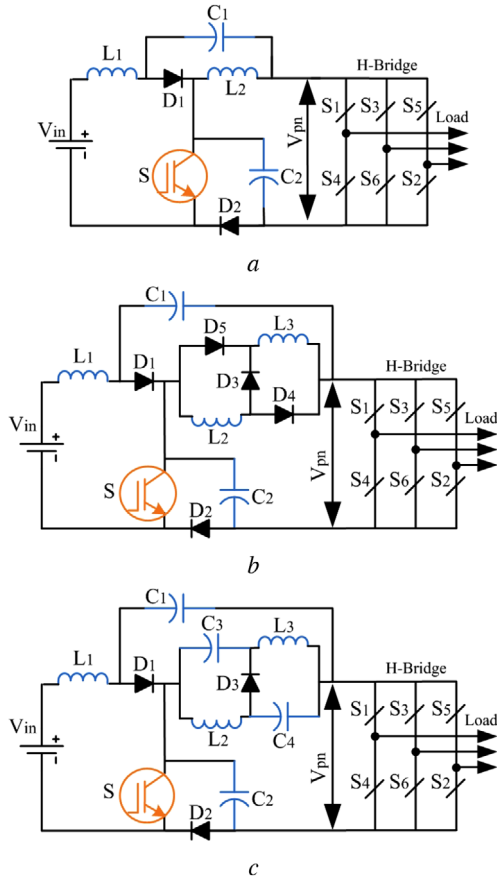
5 | CHALLENGES AND FUTURE DIRECTION

According to this survey, it can be understood that achieving all advantages in one converter design is not possible. Hence, several models are proposed to settle down the projected shortcomings of the specific ZSI/SBI-type converters. The main challenges relied on maximizing efficiency and minimizing the overall cost of the converter. A comparative cost analysis (see Figure 39) was carried out in [110] while achieving the same boost factor of 5 from the fixed DC input voltage of 35 V. In Table 8, individual components requirement and price can be found to perform the quantitative and qualitative analysis that helps to understand the practical suitability of the converter. From Table 8, it can be seen that the passive components, i.e.

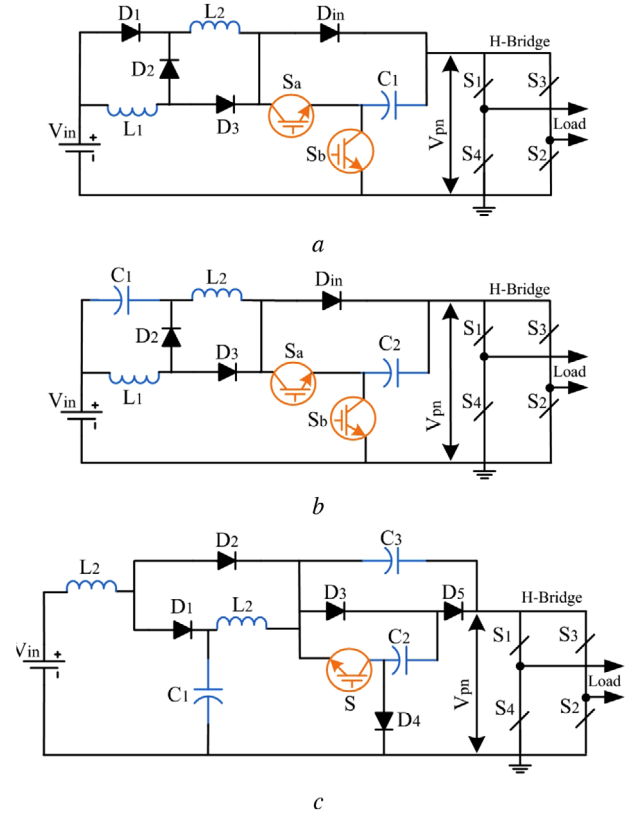
TABLE 8 Cost comparison data [110]

D_s Ref.	Capacitor (C), (Price per unit)	Inductor (L), (Price per unit)	Diode, MOSFET
0.4 [1]	$C_{1,2} = 180 \mu\text{F}/200 \text{ V}$, 1.98 \$	$L_{1,2} = 6.5 \text{ mH}/9 \text{ A}$, 7.6 \$	$5 \times S_2$, $4 \times M_1$
0.25 [30]	$C_{1,2} = 270 \mu\text{F}/160 \text{ V}$, 2.37 \$	$L_{1,4} = 2.7 \text{ mH}/8 \text{ A}$, 4.53 \$	$6 \times S_1$, $5 \times S_2$, $4 \times M_3$
0.318 [33]	$C_1 = 150 \mu\text{F}/100 \text{ V}$, 1.08 \$ $C_2 = 270 \mu\text{F}/100 \text{ V}$, 1.71 \$	$L_{1-3} = 6.5 \text{ mH}/9 \text{ A}$, 7.60 \$	$4 \times S_1$, $4 \times S_3$, $4 \times M_2$
0.444 [86]	$C_1 = 330 \mu\text{F}/200 \text{ V}$, 3.24 \$	$L_1 = 6.8 \text{ mH}/12 \text{ A}$, 20.58 \$	$1 \times S_1$, $5 \times S_2$, $5 \times M_1$
0.4 [106]	$C_1 = 220 \mu\text{F}/200 \text{ V}$, 2.19 \$	$L_1 = 6.5 \text{ mH}/9 \text{ A}$, 7.6 \$	$6 \times S_1$, $5 \times M_1$
0.444 [94]	$C_1 = 390 \mu\text{F}/160 \text{ V}$, 2.89 \$	$L_1 = 6.8 \text{ mH}/12 \text{ A}$, 20.58 \$	$1 \times S_1$, $5 \times S_2$, $5 \times M_1$
0.286 [95]	$C_1 = 390 \mu\text{F}/200 \text{ V}$, 3.42 \$	$L_1 = 4.4 \text{ mH}/12 \text{ A}$, 7.60 \$	$1 \times S_1$, $4 \times S_2$, $4 \times S_3$, $5 \times M_3$
0.286 [104]	$C_1 = 560 \mu\text{F}/250 \text{ V}$, 6.05 \$	$L_1 = 6.5 \text{ mH}/9 \text{ A}$, 7.60 \$	$1 \times S_1$, $4 \times S_2$, $4 \times S_3$, $5 \times M_3$
0.267 [104]	$C_1 = 270 \mu\text{F}/200 \text{ V}$, 2.63 \$	$L_{1,2} = 6.5 \text{ mH}/9 \text{ A}$, 7.60 \$	$1 \times S_1$, $8 \times S_2$, $5 \times M_2$
0.25 [118]	$C_1 = 220 \mu\text{F}/200 \text{ V}$, 2.62 \$	$L_1 = 6.5 \text{ mH}/9 \text{ A}$, 7.6 \$	$1 \times S_1$, $8 \times S_2$, $5 \times M_1$
0.296 [109]	$C_1 = 270 \mu\text{F}/200 \text{ V}$, 2.63 \$ $C_2 = 120 \mu\text{F}/63 \text{ V}$, 0.55 \$	$L_1 = 6.5 \text{ mH}/9 \text{ A}$, 7.6 $L_2 = 3.9 \text{ mH}/6 \text{ A}$, 3.91 \$	$4 \times S_1$, $4 \times S_2$, $5 \times M_1$
0.296 [110]	$C_1 = 270 \mu\text{F}/160 \text{ V}$, 2.37 \$ $C_2 = 180 \mu\text{F}/63 \text{ V}$, 0.74 \$	$L_1 = 6.5 \text{ mH}/9 \text{ A}$, 7.6 $L_2 = 3.9 \text{ mH}/6 \text{ A}$, 3.91 \$	$1 \times S_1$, $5 \times S_2$, $5 \times M_1$

Diode: S_1 : 1.32 \$, S_2 : 2.01 \$, S_3 : 2.51 \$; and MOSFET: M_1 : 2.77 \$, M_2 : 3.08 \$, M_3 : 5.94 \$.

**FIGURE 35** Different switched boost modified ZSI topologies (a) M-SBI, (b) (CIC) SLM-qSBI, (c) (CIC) HSLCM-qSBI

the capacitor and inductor are the two main contributors to the overall cost of a converter design. Besides, the inverter efficiency greatly depends on the number of active components used in the design. Hence, a trade-off should be ensured while config-

**FIGURE 36** Enhanced high-gain switched inductor capacitor ZSI topologies

(a) SLC-SBI-T1, (b) SLC-SBI-T2, (c) eSLC-SBI

uring the impedance network with the active and passive components. In future work, researchers can utilize active component based on GaN and SiC that may reduce the component losses and improve the efficiency, reliability, and power density of these converters [40]. According to [43], it can be predicted

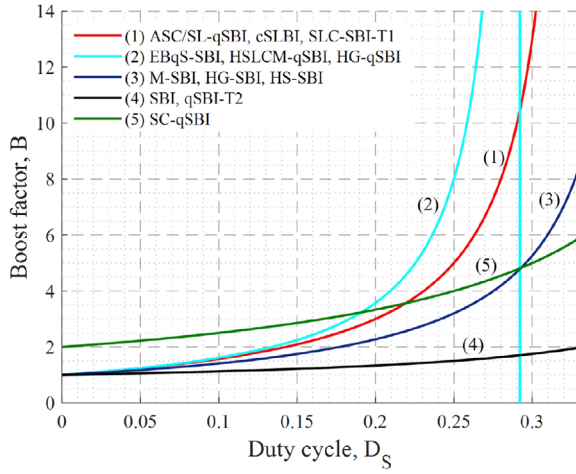


FIGURE 37 Boost factor comparison of SBIs

that the research will be expanded by considering the following objectives:

1. Promotion of the existing ZSI/SBI impedance network models in terms of boost factor, component voltage stress, total device count, and, most importantly, efficiency of the converter.

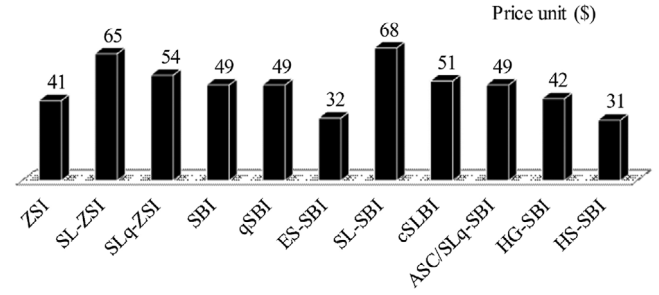


FIGURE 39 Final cost comparison [110]

2. Replacement of existing converters with ZSI networks to minimize the converter loss and improve the reliability and power quality of the overall system.
3. Investigating the practical applicability of switched ZSI/SBIs in the industrial sector.

6 | CONCLUSION

The impedance source converters with a switched Z-network have opened a wide area of research having various interesting converter properties. Therefore, it has gained much attention from the researchers over the last decades. Since the

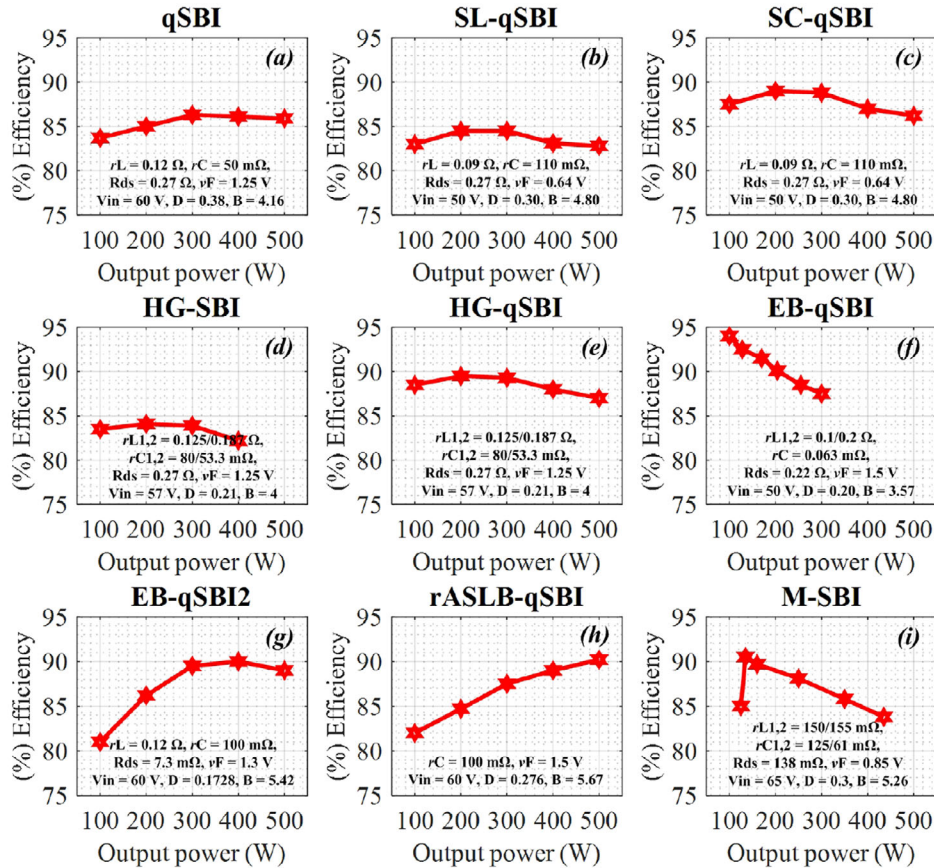


FIGURE 38 Efficiency curves of different SBIs

first introduction of the switched inductor Z-source model, a lot of efforts and contributions have been made by the expert to fetch relevant improvements and modifications. In this survey, an intensive overview on numerous switched ZSI topologies/structures/configuration/model have been addressed by framing out the basic switched inductor ZSIs, two switched inductor/capacitor ZSIs, and active switch boost ZSIs or SBIs. However, this study has been narrowed down to two-level voltage-fed DC–AC-type three-phase and single-phase switched Z-source inverters in order to provide major comparative literature. Note that all switched ZSIs or SBIs are configurable to single- or three-phase inverter regardless of their impedance configurations. All developed topologies existing in the literature are confusing despite their niche applications and advantages. This review has provided a close at-hand compilation of the recent state-of-the-art concerning specific aims and objectives. Hence, the topical picture portrayed in this review will definitely be helpful for researchers and young professionals including stakeholders from the relevant industry in order to comprehend the pros and cons of developed switched Z converters and select the most suitable one for their targeted applications.

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How to cite this article: Subhani N, Kannan R, Mahmud A, Blaabjerg F. Z-source inverter topologies with switched Z-impedance networks: A review. *IET Power Electron.* 2021;1–24.
<https://doi.org/10.1049/pel2.12064>